

# David I. August

## Curriculum Vitae

### CONTACT INFORMATION

Department of Computer Science  
Princeton University  
35 Olden Street  
Princeton, NJ 08540

Phone: (609) 258-2085  
Fax: (609) 964-1699  
august@princeton.edu  
<https://august.princeton.edu>

### EDUCATION

*University of Illinois at Urbana-Champaign, Urbana, IL*  
Ph.D. in Electrical and Computer Engineering, May 2000  
Thesis: “Systematic Compilation for Predicated Execution,” Advisor: Wen-mei W. Hwu  
M.S. in Electrical and Computer Engineering, May 1996  
Advisor: Wen-mei W. Hwu  
*Rensselaer Polytechnic Institute, Troy, NY*  
B.S. in Electrical Engineering, *summa cum laude*, May 1993

### EXPERIENCE

**Professor**, July 2012 to present; **Associate Professor**, July 2006 to June 2012; **Assistant Professor**, February 2000 to June 2006; **Lecturer**, August 1999 to January 2000  
*Department of Computer Science, Princeton University, Princeton, NJ*  
**Consultant**, August 1998-present  
*Technology and intellectual property consulting*  
**Research Intern**, May to September 1996, November 1996  
*Intel Corporation, Santa Clara, CA*  
**Research Intern**, May to August 1995  
*Hewlett Packard Laboratories, Santa Clara, CA*  
**Architecture Validation Engineer**, May to August 1994  
*Intel Corporation, Hillsboro, OR*

### RECOGNITION

- Selection of “AsmDB: Understanding and Mitigating Front-End Stalls in Warehouse-Scale Computers” for IEEE Micro’s “Top Picks” special issue “based on novelty and potential for long-term impact in the field of computer architecture” in 2019.
- Elevation to IEEE Fellow “for contributions to compilers and architectures for multicore and parallel processing systems,” 2015.
- Selection of “SWIFT: Software Implemented Fault Tolerance,” for “The Test of Time Award” at The Thirteenth International Symposium on Code Generation and Optimization (CGO), 2015.
- Selection of “DAFT: Decoupled Acyclic Fault Tolerance” by the program committee for inclusion in special issue of *The International Journal of Parallel Processing* composed of “top papers” from the 19th International Conference on Parallel Architectures and Compilation Techniques (PACT), 2010.
- Nomination of “Fault-tolerant Typed Assembly Language” as a Communications of the ACM (CACM) Research Highlight, September 2008.
- Selection of “Revisiting the Sequential Programming Model for Multi-Core” for IEEE Micro’s “Top Picks” special issue for papers “most relevant to industry and significant in contribution to the field of computer architecture” in 2007.
- Best Paper Award for “Fault-tolerant Typed Assembly Language” at the 2007 ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI), June 2007.
- Selection of “Automatic Instruction-Level Software-Only Recovery Methods” for IEEE Micro’s “Top Picks” special issue for papers “most relevant to industry and significant in contribution to the field of computer architecture” in 2006.

- Selection of “Automatic Instruction-Level Software-Only Recovery Methods” for the William C. Carter Award at the International Conference on Dependable Systems and Networks, June 2006.
- Best Paper Award for “SWIFT: Software Implemented Fault Tolerance” at the Third Annual ACM/IEEE International Symposium on Code Generation and Optimization (CGO), March 2005.
- Emerson Electric Company E. Lawrence Keyes ’51 Faculty Advancement Award, June 2003.
- Dean’s letter of recognition for teaching, Spring 2003.
- Best Paper Award for “Compiler Optimization-Space Exploration” at the First Annual ACM/IEEE International Symposium on Code Generation and Optimization (CGO), March 2003.
- Best Student Paper Award for “Microarchitectural Exploration with Liberty” at the 35th Annual ACM/IEEE International Symposium on Microarchitecture (MICRO), November 2002.
- National Science Foundation Faculty Early Career Development Award (CAREER), 2002.
- Invited presentation at University of Virginia, *Top Gun Lecture Series* recognizing “faculty on a trajectory to be research leaders of the coming decades,” December 2001.
- IBM Faculty Partnership Award, 2001-2002.
- Princeton University Research Board Award, 2001-2002.
- One of five featured by *The Chronicle of Higher Education* in its annual list of “New Ph.D.’s to Watch,” September 1999.
- Selection of “A Framework for Balancing Control Flow and Predication” by the program committee for inclusion in special issue of *The International Journal of Parallel Processing* composed of “outstanding papers” from the 30th Annual ACM/IEEE International Symposium on Microarchitecture (MICRO), 1999.
- Intel Foundation Graduate Fellowship, 1996-1997.
- Department of Defense, Office of Naval Research Graduate Fellowship, 1993-1996.
- University of Illinois Henry O. Koehler Graduate Fellowship, 1993-1994.

## ACTIVITIES

### PROGRAM CHAIR

- The 42nd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO) (with José Martínez, Cornell), 2009.
- The Fifth Annual International Symposium on Code Generation and Optimization (CGO) (with Chris J. Newburn, Intel), 2007.
- The IEEE International Conference on Computer Design (ICCD) - Computer Systems Design and Applications Track (with Mark Charney, Intel), 2003.
- The IEEE International Conference on Computer Design (ICCD) - Computer Systems Design and Applications Track (with Mark Charney, Intel), 2002.

### EDITING

- Guest Editor, IEEE Micro, special issue on “Parallelization of Sequential Code,” July 2012.
- Editorial Board, IEEE Computer Architecture Letters, 2010 - 2014.
- Associate Editor, ACM Transactions on Architecture and Code Optimization, 2006 - present.
- Guest Editor, Computer Languages, Systems and Structures special issue on “Programming Language and Compiler Support for Secure and Reliable Computing,” April 2006.

### TECHNICAL PROGRAM COMMITTEES

- The ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI), 2021.
- The CGO 2009 Test of Time Award Selection Committee, 2019
- The 16th Annual International Symposium on Code Generation and Optimization (CGO), 2018.
- The CGO 2007 Test of Time Award Selection Committee, 2017
- The 22nd International Conference on Compiler Construction (CC), 2015
- The 41st Annual IEEE/ACM International Symposium on Computer Architecture (ISCA), 2014.
- IEEE MICRO Top-Picks in Computer Architecture, 2013.
- The ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI), 2013.
- IEEE MICRO Top-Picks in Computer Architecture, 2011.
- The Fourth Workshop on Parallel Execution of Sequential Programs on Multi-core Architectures (PE-SPMA), 2011

- The 11th International Symposium on Advanced Parallel Processing Technologies (APPT), 2011
- The First International Workshop on Future Architectural Support for Parallel Programming (FASPP), 2011
- The 16th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2011.
- The 43rd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), 2010.
- The Third Workshop on Emerging Applications and Many-core Architecture (EAMA), 2010.
- The Sixth Workshop on Modeling, Benchmarking and Simulation (MoBS), 2010.
- The First Workshop on Accelerators for High-performance Architectures (WAHA), 2009
- The Fifth IEEE International Symposium on Workload Characterization (IISWC), 2009.
- The ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI), 2008.
- IEEE MICRO Top-Picks in Computer Architecture, 2007.
- The Sixth Annual Workshop on Duplicating, Deconstructing, and Debunking (WDDD), 2007.
- The ACM International Conference on Computing Frontiers (CF), 2007.
- The 34th Annual IEEE/ACM International Symposium on Computer Architecture (ISCA), 2007.
- The 39th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), 2006.
- The International Conference on High Performance Embedded Architectures and Compilers (HiPEAC), 2006.
- The Workshop on Introspective Architectures (WISA), 2006.
- The 15th International Conference on Parallel Architectures and Compilation Techniques (PACT), 2006.
- The Second Workshop on Modeling, Benchmarking and Simulation (MoBS), 2006.
- The 10th Workshop on Interaction between Compilers and Computer Architectures (INTERACT), 2006.
- The IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2006.
- The 32nd Annual IEEE/ACM International Symposium on Computer Architecture (ISCA), 2005.
- The Workshop on Modeling, Benchmarking and Simulation (MoBS), 2005.
- The IEEE/ACM International Conference on Computer Aided Design (ICCAD), 2005.
- The International Conference on High Performance Embedded Architectures and Compilers (HiPEAC), 2005.
- The Third Annual International Symposium on Code Generation and Optimization (CGO), 2005.
- The International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), 2004.
- The IEEE International Conference on Computer Design (ICCD) - Computer Systems Design and Applications Track, 2004.
- The IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2004.
- The Second Annual International Symposium on Code Generation and Optimization (CGO), 2004.
- The 30th Annual IEEE/ACM International Symposium on Computer Architecture (ISCA), 2003.
- The First Annual International Symposium on Code Generation and Optimization (CGO), 2003.
- The IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2003.
- The 35th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), 2002.
- The ACM Workshop on Languages, Compilers, and Tools for Embedded Systems (LCTES), 2002.
- The ACM International Conference on Measurement and Modeling of Computer Systems (SIGMETRICS), 2002.
- The 6th Workshop on Interaction between Compilers and Computer Architectures (INTERACT), 2002.
- The First Annual Workshop on Explicitly Parallel Instruction Computer Architectures and Compiler Technology (EPIC), 2001.
- The ACM Workshop on Languages, Compilers, and Tools for Embedded Systems (LCTES), 2001.
- The IEEE International Conference on Computer Design (ICCD), 2001.
- The 7th International IEEE Symposium on High-Performance Computer Architecture (HPCA), 2000.
- The IEEE International Conference on Computer Design (ICCD), 2000.

#### CONFERENCE ORGANIZING AND STEERING COMMITTEES

- Steering Committee, The International Symposium on Code Generation and Optimization (CGO), 2007-2010.
- General Chair, The Fourth Annual International Symposium on Code Generation and Optimization (CGO), 2006.
- Publications Chair, The IEEE International Symposium on Performance Analysis of Systems and Soft-

ware (ISPASS), 2003.

- Finance Chair, The Second Annual International Symposium on Code Generation and Optimization (CGO), 2003
- General Chair, The Second Annual Workshop on Explicitly Parallel Instruction Computer Architectures and Compiler Technology (EPIC), 2002.

#### TECHNICAL PANELS

- Panelist, “Advancing Computer Systems without Technology Progress,” DARPA Information Science and Technology (ISAT) Workshop, March 2012.
- Panelist, “Freedom from the Tyranny of Parallel Programming,” Workshop on Deterministic Multiprocessing and Parallel Programming (WoDet), November 2009.
- Panelist, “Programming for Multi-core Processors (OR NOT?)” Second Workshop on Computer Architecture Research Directions (CARD) held in conjunction with International Symposium on Computer Architecture (ISCA), June 2009.
- Panelist, “Are New Programming Languages Needed to Exploit Manycore Architectures?” Microsoft Research Faculty Summit, July 2007.
- Panelist, “Programming Languages/Models and Compiler Technologies,” Manycore Computing Workshop held in conjunction with the International Conference on Supercomputing (ICS), June 2007.
- Panelist, “Are New Languages Necessary for Multicore,” The Fifth International Symposium on Code Generation and Optimization (CGO), March 2007.
- Panelist, “Directions in Multi-Core Research,” Microsoft Corporation, Redmond, WA, January 2007.
- Panelist, “What should architects know about compilers and systems software?” The Computing Research Association’s Committee on the Status of Women (CRA-W) and the Coalition to Diversify Computing (CDC) Computer Architecture Summer School, 2006.
- Panelist, “Design Methodologies for Future Processor Chips,” The Second Workshop on Modeling, Benchmarking and Simulation held in conjunction with the 33rd International Symposium on Computer Architecture (ISCA), 2006.
- Panelist, “Simulation Methodology,” Third Annual Workshop on Duplicating, Deconstructing, and Debunking (WDDD) held in conjunction with International Symposium on Computer Architecture (ISCA), 2004.
- Panelist, “Emerging Issues with Simulation Technology” NSF-Sponsored Workshop, Austin, TX, December 2001.

#### FUNDING PANELS

- National Science Foundation Secure and Trusted Cyberspace (SaTC) Faculty Early Career Development (CAREER) Panel
- National Science Foundation Secure and Trusted Cyberspace (SaTC) Computer and Information Science and Engineering Research Initiation Initiative (CRII) Panel
- National Science Foundation Secure and Trusted Cyberspace Panel (SaTC)
- National Science Foundation Software and Hardware Foundations Panel (SHF)
- National Science Foundation Computing Systems Research Panel (CSR) (2 times)
- National Science Foundation Computer Systems Architecture Panel (CSA)
- National Science Foundation Information Technology Research Panel (ITR)
- National Science Foundation Next Generation Software Panel (NGS)

#### TUTORIALS

- “Next Generation Automatic Parallelization,” presented at the Eighth International Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems, Fiuggi, Italy, June 2012.
- “Fault Tolerant Computing,” Summer School on Language-Based Techniques for Integrating with the External World, July 2007.
- “Structural Simulation,” presented at the First International Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems, L’Aquila, Italy, June 2005.

- “Using The Liberty Simulation Environment with emphasis on validated OS-level simulation,” presented at the 11th International Conference on Architectural Support for Programming Languages and Operating Systems in Boston, MA, October 2004.
- “The Liberty Simulation Environment, Version 1.0,” presented at the 36th International Symposium on Microarchitecture in San Diego, CA, December 2003.
- “Architectural Exploration with Liberty,” presented at the International Symposium on Microarchitecture in Austin, TX, December 2001.
- “Future Technologies and Markets for Programmable Platform-Based Design,” presented at IP/SoC 2001 in Santa Clara, CA, March 2001.

## INVITED TALKS

- Keynote: “Thoughts on Restoring Computing’s Former Glory,” presented at the 2012 Compiler, Architecture and Tools Day, Haifa, Israel, November 2012.
- Keynote: “Restoring Computing’s Former Glory,” presented at the 2012 Architecture of Computing Systems Conference, Munich, Germany, March 2012.
- “A Roadmap to Restoring Computing’s Former Glory,” presented at the HiPEAC Industrial Workshop, High-Performance and Embedded Computing, Charmonix, France, April 2011.
- Keynote: “Indistinguishable from Magic,” presented at the 16th Workshop on Compiler Techniques for High-Performance and Embedded Computing, Taipei, Taiwan, May 2010.
- Keynote: “Parallelism for Multicore,” presented at the 2009 Workshop on Parallel Execution of Sequential Programs on Multi-core Architectures held in conjunction with 36th International Symposium on Computer Architecture, June, 2009.
- “Parallelism for Multicore,” presented at the New Jersey Programming Languages Seminar and Princeton Computer Architecture Research Day, March, 2009.
- “Addressing the Multicore Problem,” presented at the Princeton Innovation Forum, March, 2009.
- “Automatic Thread Extraction from Sequential Programs,” presented at Indian Institute of Science, March, 2008.
- “The Multicore Challenge,” DARPA Information Processing Technology Office Futures Panel, December 2007.
- “Automatic Thread Extraction from Sequential Programs,” presented at Microsoft Research Faculty Summit, 2007.
- “Liberating Threads from Sequential Programs,” presented at Purdue University, November 2006.
- “The Jericho Project,” presented at the Workshop on Design, Architecture and Simulation of Chip Multi-Processors, November 2005.
- “Liberating Threads from Sequential Programs,” presented at Intel Microprocessor Laboratories, Hewlett-Packard Laboratories, Sun Microsystems Research Laboratories, INRIA Futurs, Cornell University, Carnegie Mellon University, and Massachusetts Institute of Technology, March-April 2005.
- “Liberating Threads from Sequential Programs,” presented at the New Jersey Programming Languages Seminar, February 2005.
- “Liberty Compiler Research,” presented at IBM T. J. Watson Research Center, April 2004.
- “Liberty Research,” presented at Infineon Corporation and Aachen University, February 2004.
- “Architectural Exploration with Liberty,” presented at the Intel High-Level Design Research Forum, November 2002.
- “Optimization-Space Exploration,” presented at Intel Microprocessor Research Laboratories, Hewlett-Packard Laboratories, and Sun Microsystems Research Laboratories, August 2002.
- “Architectural Exploration with Liberty,” presented at IBM T. J. Watson Research Center, July 2002.
- “Liberty Compiler and Architecture Research,” presented at University of Texas at Austin, April 2002.
- “Architectural Exploration with Liberty,” presented at University of Virginia, *Top Gun Lecture Series* recognizing “faculty on a trajectory to be research leaders of the coming decades,” December 2001.
- “Architectural Exploration with Liberty,” presented at Intel Microprocessor Laboratories, Hewlett-Packard Laboratories, and Sun Microsystems Research Laboratories, May 2001.
- “Architectural Exploration with Liberty,” presented at University of Toronto, Distinguished Lecture Series, May 2001.
- “Systematic Compilation for Predicated Execution,” presented at IBM Tokyo Research Laboratories, Rice University, and University of Illinois at Urbana/Champaign, January-August 2000.
- “Systematic Program Decision Logic Optimization Using Predication,” presented at Intel Microprocessor

Research Laboratories, April 1999.

- “Enabling Compiler Technology for Predication,” presented at The Swiss Federal Institute of Technology of Lausanne (École Polytechnique Fédérale de Lausanne), February 1999.
- “Enabling Compiler Technology for Predication,” presented at Compaq Corporation, November 1998.
- “A Global Predication Compilation Framework,” presented at Microsoft Research, November 1998.
- “Predicated Microprocessor Architectures and Their Enabling Compiler Technology,” presented at Silicon Graphics, February 1998.
- “Next Generation Predication Support in the IMPACT Compiler,” presented at The Intel Foundation Fellowship Forum, November 1996.
- “Predicated Execution Architectures: New Research Results and Directions,” presented at The Intel Microprocessor Research Forum, October 1995.

## GRANTS

- “Practical, Efficient, and Unified I-Cache and BTB Prefetching for Scale-out Workloads,” Google Research Award, \$75,000, November 2019.
- “The Whole Program Critical Path Approach to Parallelism,” National Science Foundation, Software and Hardware Foundations (SHF) (CCF 1814654), \$500,000, October 2018 to September 2021. (Sole PI)
- “Practical, Efficient, and Unified I-Cache and BTB Prefetching for Scale-out Workloads,” Google Research Award, \$87,893, February 2018.
- “TrustGuard-secured Computing Devices,” The Princeton University Intellectual Property Accelerator Fund, \$100,000, January 2017. (Sole PI)
- “An Architecture for Restoring Trust in Our Personal Computing Systems,” National Science Foundation, Secure and Trustworthy Cyberspace (SaTC) (CNS 1441650), \$500,000, September 2014 to August 2017. (Sole PI)
- “A Framework for Portable Parallel Performance,” National Science Foundation, Exploiting Parallelism and Scalability (XPS) (CCF 1439085), \$300,000, August 2014 to July 2017. (Sole PI)
- “A Platform for Data-Parallel GPU Computing at Princeton,” National Science Foundation, Computing Research Infrastructure (CRI) Program (CNS 1205613), \$350,000, August 2012. (PI with 3 Co-PIs)
- “PRACTICE: Power-Reducing Adaptive Computing Technologies: Intelligent, Cross-layer, and Efficient,” United States Department of Defense (DOD), Defense Advanced Research Projects Agency (DARPA), Power Efficiency Revolution For Embedded Computing Technologies (PERFECT) Program, \$10,928,472, January 2012 to August 2015. (PI with 3 others)
- “A Platform for Data-Parallel GPU Computing at Princeton,” National Science Foundation, Computing Research Infrastructure (CRI) Program (CNS 1205613), \$350,000, August 2012. (PI with 3 Co-PIs)
- “Accelerating the Pace of Research (at Princeton),” Dean for Research Fund, \$50,000, April 2012.
- “Automatic Parallelization for GPUs,” NVIDIA Corporation Academic Partnership Award, \$25,000, December 2010.
- “Accelerating the Pace of Research through Implicitly Parallel Programming,” National Science Foundation, Software Infrastructure for Sustained Innovation Scientific (SI<sup>2</sup>) Software Integration (SSI) Program (OCI 1047879), \$1,740,314, October 2010 to September 2014. (PI with Walker)
- “Greater Philadelphia Innovation Cluster (GPIC) for Energy Efficient Buildings,” United States Energy Regional Innovation Cluster (E-RIC) Initiative, \$3,499,994 (\$129,000,000 overall), October 2010 to September 2015. (Princeton University PI with 4 Co-PIs)
- “SPARCHS: Symbiotic, Polymorphic, Autotomic, Resilient, Clean-Slate, Host Security,” United States Department of Defense (DOD), Defense Advanced Research Projects Agency (DARPA), Clean-slate design of Resilient, Adaptive, Secure Hosts (CRASH) Program, \$6,424,180, September 2010 to September 2014. (PI with 4 others)
- “Scaling the Implicitly Parallel Programming Model with Lifelong Thread Extraction and Dynamic Adaptation,” National Science Foundation, Computer Systems Research (CSR) Program (CNS 0964328), \$1,199,998, May 2010 to April 2013. (PI with Hazelwood and Mahlke)
- “AESOP: Adaptive Environment for Supercompiling with Optimized Parallelism,” United States Department of Defense (DOD), Defense Advanced Research Projects Agency (DARPA), Architecture-Aware Compiler Environment (AACE) Program, \$11,572,332, September 2009 to January 2013. (PI with 4 others)
- “Implicitly Parallel Programming with Dynamic Execution,” LG Electronics, \$40,000, November 2009.

- “Hierarchical Latency and Throughput Optimization of Parallel Applications,” Google Research Award, \$50,000, November 2009.
- “A Hybrid Approach for Petascale Computing: Accelerating Scientific Research,” National Science Foundation, Small Grants for Exploratory Research (SGER) Program (OCI 0849512), \$102,562, June 2009 to May 2010. (PI with Li and Ostriker)
- “Revisiting the Sequential Programming Model for Multicore Systems,” National Science Foundation, Computing Processes and Artifacts (CPA) Program (CCF 0811580), \$150,000, September 2008 to August 2009. (PI with Hazelwood and Mahlke)
- “Automatically Parallelizing Legacy Binary Code for Multi-Core Architectures via Extraction of Self-Similarity,” United States Department of Defense (DOD), Defense Advanced Research Projects Agency (DARPA), \$300,000, September 2008 to August 2009. (PI with Locasto, Sethumadhavan, and Stolfo)
- “Liberating Threads from Sequential Programs,” Gigascale Silicon Research Center, \$357,000, September 2006 to August 2009. (Sole PI)
- “Well-typed Trustworthy Computing in the Presence of Transient Faults,” National Science Foundation, CyberTrust Program (CNS 0627650), \$1,100,000, September 2006 to June 2010. (Co-PI with Walker, Appel, Clark, and Martonosi)
- “Software-Modulated Fault Tolerance,” National Science Foundation, Computer Systems Research (CSR) Program (CNS 0615250), \$320,000, July 2006 to June 2009. (Sole PI)
- “A Viable Approach to Compiling Sequential Codes for CMPs,” Microsoft Corporation, \$50,000, April 2006.
- “Flow-Based Computer Systems Support for Synergistic Hardware-Software Management of Embedded Systems,” National Science Foundation, Computer Systems Research (CSR) Program (CNS 0509402), \$500,000, September 2005 to August 2009. (Co-PI with Li, Martonosi, and Pe)
- “User-centric Information Flow Security,” Intel Corporation, \$120,000, August 2005 to July 2008.
- “Threading the CMP Needle with Fibers and Frays,” The Microelectronics Advanced Research Corporation (MARCO), \$122,500, April 2005 to August 2006. (Sole PI)
- “International Modular Simulation Research,” Direction des Relations Européennes et Internationales (DREI), Programme INRIA “Equipes Associées”, €60,000, January 2005 to December 2007. (Co-PI)
- “A Structural and Composable Framework for MP Systems,” Intel Corporation, \$135,000, September 2003.
- “Structural and Composable Performance Simulation of Complex Systems,” National Science Foundation, Next Generation Software (NGS) Program (CNS 0305617), \$1,101,503, September 2003 to August 2006. (PI with Malik, Pai, and Peh)
- Emerson Electric Co. E. Lawrence Keyes ’51 Award, \$30,000, June 2003.
- Xilinx Equipment Grant, \$46,300, June 2003.
- “Addressing The Mapping Problem,” Infineon Corporation, \$100,000, November 2003.
- “Optimization-Space Exploration,” Intel Corporation, \$53,000, March 2002.
- “Systematic Design-Space Exploration,” National Science Foundation, Faculty Early Career Development Award (CAREER) (CCF 0133712), \$357,130, January 2002 to December 2006. (Sole PI)
- “EPIC Compiler and Architecture Research,” Hewlett-Packard and Intel Corporation Itanium Processor Family Equipment Grant, \$64,960, November 2001. (Coordinated university wide grant of \$242,157.)
- “Analysis Tools for Network Processors,” IBM Corporation, \$30,000, June 2001.
- “Memory Shape and Flow Determination,” Intel Corporation, \$53,000, March 2001.
- “Modern Embedded Systems: Compilers, Architectures, and Languages (MESCAL),” Gigascale Silicon Research Center, \$350,000, January 2001 to December 2003. (Sole PI)
- “Ascertaining Runtime Branch Characteristics through Algebraic Analysis of Programs,” National Science Foundation, Information Technology Research (ITR) Program (CCF 0082630), \$310,000, September 2000 to August 2002. (PI with Clark and Skadron)

## OUTREACH

- Presenter of dozens of STEM demonstrations to early elementary public school students. Students, teachers, and parents report that these demonstrations have made a significant impression on young students.

## UNIVERSITY SERVICE

- Committee on Discipline, 2016-2020
- University Committee on Library and Computing, 2017-2021
- Computer Science Class of 2018 BSE Advisor
- Princeton University Research Computing Advisory Group
- Computer Science Department's Instructor Coordinator, 2014-2015
- Andlinger Center for Energy and the Environment Space Committee
- Computer Science Department's Instructor Recruiting Committee, 2012-2015
- Princeton Institute for Computational Science and Engineering (PICSciE) Faculty Committee
- Computer Science Department's Computing Infrastructure Advisory Group
- Computer Science Department's Renovation Advisory Group
- Coordinator of various joint activities with the Department of Electrical Engineering
- Computer Science Department's Diversity Task Force
- Class of 2004, 2005, 2006, 2007, 2008, 2009, 2014, 2015, 2016, 2022, 2023, 2024 BSE Freshmen Advising
- Mathey College Faculty Fellow
- University Committee on Library and Computing, 2011-2014
- Associate Chair, Computer Science Department, 2007-2008
- University Committee on Examinations and Standing, 2006-2008
- University Committee on Committees, 2002-2005
- Computer Science Class of 2004 BSE Advisor
- School of Engineering and Applied Science *Ad Hoc* Committee on the Computing Requirement
- Co-leader School of Engineering and Applied Science Strategic Planning Executive Committee for Focus on the Faculty

## TEACHING

- COS-126: Introduction to Computer Science (Dean's letter of recognition for teaching)
- COS-217: Introduction to Programming Systems
- COS-320: Compiler Implementation
- COS-375: Introduction to Computer Architecture
- COS-598: Parallelism
- COS-598: Feedback-Directed Optimization
- COS-598: Computer Architecture Research Infrastructure Development
- COS-598: Synergistic Hardware-Compiler Architecture Design
- COS-598: Topics in Compiler Construction
- COS-598: Securing Hardware

## STUDENTS

### CURRENT DOCTORAL STUDENTS

Nayana Prasad Nagendra (year 6), Hansen Zhang (year 6), Sotiris Apostolakis (year 5), Bhargav Reddy Godala (year 2), Gregory Chan (year 2), Ziyang Xu (year 2)

### COMPLETED DEGREES

Jordan Fix

Ph.D. Thesis: Hardware MultiThreaded Transactions: Enabling Speculative MultiThreaded Pipeline Parallelization For Complex Programs

First Position: Facebook

Stephen Beard

Ph.D. Thesis: TrustGuard: A Model for Practical Trust in Real Systems

First Position: Founder at Start-up

Feng Liu

Ph.D. Thesis: Static and Dynamic Instruction Mapping for Spatial Architectures

First Position: Databricks



Soumyadeep Ghosh  
Ph.D. Thesis: TrustGuard: A Containment Architecture with Verified Output  
First Position: Founder at Start-up

Heejin Ahn  
Master of Engineering Degree  
First Position: Google

Nick Johnson  
Ph.D. Thesis: Static Dependence Analysis in an Infrastructure for Automatic Parallelization  
First Position: D. E. Shaw Research

Taewook Oh  
Ph.D. Thesis: Automatic Exploitation of Input Parallelism  
First Position: Facebook

Thomas Jablin  
Ph.D. Thesis: Automatic Parallelization for GPUs  
First Position: University of Illinois

Prakash Prabhu  
Ph.D. Thesis: Semantic Language Extensions for Implicit Parallel Programming  
First Position: Google

Jialu Huang  
Ph.D. Thesis: Automatically Exploiting Cross-Invocation Parallelism Using Runtime Information  
First Position: Goldman Sachs

Hanjun Kim  
Ph.D. Thesis: ASAP: Automatic Speculative Acyclic Parallelization for Clusters  
First Position: Assistant Professor at Pohang University of Science and Technology

Arun Raman  
Ph.D. Thesis: A System for Flexible Parallel Execution  
First Position: Intel

Yun Zhang  
Ph.D. Thesis: Runtime Speculative Software-Only Fault Tolerance  
First Position: Goldman Sachs

Matthew Zoufaly  
Master of Engineering Degree  
First Position: Partner at Start-up

Jack Tzu-Han Hung  
Master of Engineering Degree  
First Position: Intel

Easwaran Raman  
Ph.D. Thesis: Parallelization Techniques with Improved Dependence Handling  
First Position: Google

Thomas Mason  
Master of Engineering Degree  
First Position: Johns Hopkins University Applied Physics Laboratory

Matthew Bridges  
Ph.D. Thesis: The VELOCITY Compiler: Extracting Efficient Multicore Execution from Legacy Sequential Codes  
First Position: Google

Bolei Guo  
Ph.D. Thesis: Shape Analysis with Inductive Recursion Synthesis  
First Position: JPMorgan

Neil Vachharajani

Ph.D. Thesis: Intelligent Speculation for Pipelined Multithreading

First Position: Google

Guilherme Ottoni

Ph.D. Thesis: Global Instruction Scheduling for Multi-Threaded Architectures

First Position: Intel Research

George A. Reis

Ph.D. Thesis: Software Modulated Fault Tolerance

First Position: Google

Ram Rangan

Ph.D. Thesis: Pipelined Multithreading Transformations and Support Mechanisms

First Position: IBM Austin Research Laboratory

Spyridon Triantafyllis

Ph.D. Thesis: Eliminating Conventional Restrictions on Compiler Optimization

First Position: D. E. Shaw Research

David A. Penry

Ph.D. Thesis: Microarchitecture Modeling for Design-space Exploration

First Position: Assistant Professor at Brigham Young University

Manish Vachharajani, co-advised with Sharad Malik

Ph.D. Thesis: Microarchitecture Modeling for Design-space Exploration

First Position: Assistant Professor at University of Colorado, Boulder

Jason Blome

Master of Engineering Degree

First Position: Ph.D. candidate at University of Michigan, Ann Arbor

## PUBLICATIONS

### BOOK CHAPTERS

- [1] David I. August, Jialu Huang, Thomas B. Jablin, Hanjun Kim, Thomas R. Mason, Prakash Prabhu, Arun Raman, and Yun Zhang, "Automatic Extraction of Parallelism from Sequential Code," in *Fundamentals of Multicore Software Development* edited by Ali-Reza Adl-Tabatabai, Chapman Hall / CRC Press, December 2011. (ISBN: 978-1439812730)
- [2] Arun Raman and David I. August, "EPIC Processors," in *Encyclopedia of Parallel Computing* edited by David Padua, Springer, November 2011. (ISBN: 978-0387098449)
- [3] David I. August, Veerle Desmet, Silvain Girbal, Daniel Gracia Prez, and Olivier Temam, "Structural Simulation for Architecture Exploration," in *Processor and System-on-Chip Simulation* edited by Rainer Leupers and Olivier Temam, Springer, September 2010. (ISBN: 978-1441961747)
- [4] Neil Vachharajani and David I. August, "Speculation," in *Encyclopedia of Computer Science and Engineering* edited by Benjamin W. Wah, John Wiley Sons, Inc., January 2009. (ISBN: 978-0471383932)
- [5] Easwaran Raman and David I. August, "Optimizations for the Memory Hierarchy," in *Compiler Design Handbook* edited by Y. N. Srikant, CRC Press, December 2007. (ISBN: 978-1420043822)
- [6] David I. August, "Branch Predication," in *Speculative Execution in High Performance Computer Architectures* edited by D. Kaeli and P.-C. Yew, CRC Press, May 2005. (ISBN: 978-1584884477)

### REFEREED JOURNAL PUBLICATIONS

- [7] Nayana P. Nagendra, Grant Ayers, David I. August, Hyoun K. Cho, Svilen Kanev, Christos Kozyrakis, Trivikram Krishnamurthy, Heiner Litz, Tipp Moseley, and Parthasarathy Ranganathan, "AsmDB: Understanding and Mitigating Front-End Stalls in Warehouse-Scale Computers," in *IEEE Micro*, May 2020.  
**IEEE Micro's "Top Picks" special issue "based on novelty and potential for long-term impact in the field of computer architecture" in 2019.**

- [8] Yun Zhang, Jae W. Lee, Nick P. Johnson, and David I. August, “DAFT: Decoupled Acyclic Fault Tolerance,” in *The International Journal of Parallel Programming (IJPP)*, February 2012. Invited. **Special issue composed of “top papers” selected by the Program Committee of the 19th International Conference on Parallel Architectures and Compilation Techniques.**
- [9] Arvind, David I. August, Keshav Pingali, Derek Chiou, Resit Sendag, and Joshua J. Yi, “Programming Multicores: Do Applications Programmers Need to Write Explicitly Parallel Programs?,” in *IEEE Micro*, May 2010.
- [10] Ram Rangan, Neil Vachharajani, Guilherme Ottoni, and David I. August, “Performance Scalability of Decoupled Software Pipelining,” in *ACM Transactions on Architecture and Code Optimization (TACO)*, August 2008.
- [11] Matthew J. Bridges, Neil Vachharajani, Yun Zhang, Thomas B. Jablin, and David I. August, “Revisiting the Sequential Programming Model for the Multicore Era,” in *IEEE Micro*, January 2008. **IEEE Micro’s “Top Picks” special issue for papers “most relevant to industry and significant in contribution to the field of computer architecture” in 2007.**
- [12] David I. August, Jonathan Chang, Sylvain Girbal, Daniel Gracia-Perez, Gilles Mouchard, David Penry, Olivier Temam, and Neil Vachharajani, “UNISIM: An Open Simulation Environment and Library for Complex Architecture Design and Collaborative Development,” in *IEEE Computer Architecture Letters (CAL)*, September 2007.
- [13] George A. Reis, Jonathan Chang, and David I. August, “Automatic Instruction-Level Software-Only Recovery Methods,” in *IEEE Micro*, January 2007. **IEEE Micro’s “Top Picks” special issue for papers “most relevant to industry and significant in contribution to the field of computer architecture” in 2006.**
- [14] Manish Vachharajani, Neil Vachharajani, David A. Penry, Jason A. Blome, Sharad Malik, and David I. August, “The Liberty Simulation Environment: A Deliberate Approach to High-Level System Modeling,” in *ACM Transactions on Computer Systems (TOCS)*, August 2006.
- [15] George A. Reis, Jonathan Chang, Neil Vachharajani, Ram Rangan, David I. August, and Shubhendu S. Mukherjee, “Software-Controlled Fault Tolerance,” in *ACM Transactions on Architecture and Code Optimization (TACO)*, December 2005.
- [16] Guilherme Ottoni, Ram Rangan, Adam Stoler, Matthew J. Bridges, and David I. August, “From Sequential Programs to Concurrent Threads,” in *IEEE Computer Architecture Letters (CAL)*, June 2005.
- [17] David I. August, Sharad Malik, Li-Shiuan Peh, Vijay Pai, Manish Vachharajani, and Paul Willmann, “Achieving Structural and Composable Modeling of Complex Systems,” in *The International Journal of Parallel Programming (IJPP)*, June 2005. Invited.
- [18] Spyridon Triantafyllis, Manish Vachharajani, and David I. August, “Compiler Optimization-Space Exploration,” in *The Journal of Instruction-level Parallelism (JILP)*, February 2005.
- [19] Manish Vachharajani, Neil Vachharajani, David A. Penry, Jason Blome, and David I. August, “The Liberty Simulation Environment, Version 1.0,” in *Performance Evaluation Review: Special Issue on Tools for Architecture Research (PER)*, March 2004. Invited.
- [20] Kevin Skadron, Margaret Martonosi, David I. August, Mark D. Hill, David J. Lilja, and Vijay S. Pai, “Challenges in Computer Architecture Evaluation,” in *IEEE Computer*, August 2003.
- [21] David I. August, Kurt Keutzer, Sharad Malik, and A. Richard Newton, “A Disciplined Approach to the Development of Platform Architectures,” in *Microelectronics Journal*, November 2002. Invited.
- [22] Wen-mei W. Hwu, David I. August, and John W. Sias, “Program Decision Logic Optimization using Predication and Control Speculation,” in *Proceedings of the IEEE*, November 2001.

- [23] David I. August, Wen-mei W. Hwu, and Scott A. Mahlke, “The Partial Reverse If-Conversion Framework for Balancing Control Flow and Predication,” in *International Journal of Parallel Programming (IJPP)*, October 1999. Invited.  
**Special issue composed of “outstanding papers” selected by the Program Committee of the 30th Annual ACM/IEEE International Symposium on Microarchitecture.**
- [24] Wen-mei W. Hwu, Richard E. Hank, David M. Gallagher, Scott A. Mahlke, Daniel M. Lavery, Grant E. Haab, John C. Gyllenhaal, and David I. August, “Compiler Technology for Future Microprocessors,” in *Proceedings of the IEEE*, December 1995.

#### REFEREED CONFERENCE PUBLICATIONS

- [25] Sotiris Apostolakis, Ziyang Xu, Zujun Tan, Greg Chan, Simone Campanoni, and David I. August, “SCAF: A Speculation-Aware Collaborative Dependence Analysis Framework,” in *Proceedings of the 41st ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, June 2020.  
**Awarded all top ACM Reproducibility Badges offered by the Artifact Evaluation Committee.**
- [26] Sotiris Apostolakis, Ziyang Xu, Greg Chan, Simone Campanoni, and David I. August, “Perspective: A Sensible Approach to Speculative Automatic Parallelization,” in *Proceedings of the Twenty-Fifth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March 2020.  
**Awarded all top ACM Reproducibility Badges offered by the Artifact Evaluation Committee.**
- [27] Grant Ayers, Nayana P. Nagendra, David I. August, Hyoun K. Cho, Svilen Kanev, Christos Kozyrakis, Trivikram Krishnamurthy, Heiner Litz, Tipp Moseley, and Parthasarathy Ranganathan, “AsmDB: Understanding and Mitigating Front-End Stalls in Warehouse-Scale Computers,” in *Proceedings of the 46th International Symposium on Computer Architecture (ISCA)*, June 2019.  
**Selected for IEEE Micro’s “Top Picks” special issue “based on novelty and potential for long-term impact in the field of computer architecture” in 2019.**
- [28] Hansen Zhang, Soumyadeep Ghosh, Jordan Fix, Sotiris Apostolakis, Stephen R. Beard, Nayana P. Nagendra, Taewook Oh, and David I. August, “Architectural Support for Containment-based Security,” in *Proceedings of the Twenty-Fourth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, April 2019.
- [29] Prakash Prabhu, Stephen R. Beard, Sotiris Apostolakis, Ayal Zaks, and David I. August, “MemoDyn: Exploiting Weakly Consistent Data Structures for Dynamic Parallel Memoization,” in *Proceedings of the 27th International Conference on Parallel Architectures and Compilation Techniques (PACT)*, November 2018.
- [30] Jordan Fix, Nayana P. Nagendra, Sotiris Apostolakis, Hansen Zhang, Sophie Qiu, and David I. August, “Hardware MultiThreaded Transactions,” in *Proceedings of the Twenty-Third International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March 2018.
- [31] Taewook Oh, Stephen R. Beard, Nick P. Johnson, Sergiy Popovych, and David I. August, “A Generalized Framework for Automatic Scripting Language Parallelization,” in *Proceedings of the 26th International Conference on Parallel Architectures and Compilation Techniques (PACT)*, September 2017.
- [32] Nick P. Johnson, Jordan Fix, Taewook Oh, Stephen R. Beard, Thomas B. Jablin, and David I. August, “A Collaborative Dependence Analysis Framework,” in *Proceedings of the 2017 International Symposium on Code Generation and Optimization (CGO)*, February 2017.  
**Highest ranked paper in double-blind review process.**
- [33] Jialu Huang, Prakash Prabhu, Thomas B. Jablin, Soumyadeep Ghosh, Sotiris Apostolakis, Jae W. Lee, and David I. August, “Speculatively Exploiting Cross-Invocation Parallelism,” in *Proceedings of the 25th International Conference on Parallel Architectures and Compilation Techniques (PACT)*, September 2016.

- [34] Feng Liu, Heejin Ahn, Stephen R. Beard, Taewook Oh, and David I. August, “DynaSpAM: Dynamic Spatial Architecture Mapping using Out of Order Instruction Schedules,” in *Proceedings of the 42nd International Symposium on Computer Architecture (ISCA)*, June 2015.
- [35] Feng Liu, Soumyadeep Ghosh, Nick P. Johnson, and David I. August, “CGPA: Coarse-Grained Pipelined Accelerators,” in *The Design Automation Conference (DAC)*, June 2014.
- [36] Nick P. Johnson, Taewook Oh, Ayal Zaks, and David I. August, “Fast Condensation of the Program Dependence Graph,” in *Proceedings of the 34th ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, June 2013.
- [37] Taewook Oh, Hanjun Kim, Nick P. Johnson, Jae W. Lee, and David I. August, “Practical Automatic Loop Specialization,” in *Proceedings of the Eighteenth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March 2013.
- [38] Jialu Huang, Thomas B. Jablin, Stephen R. Beard, Nick P. Johnson, and David I. August, “Automatically Exploiting Cross-Invocation Parallelism Using Runtime Information,” in *Proceedings of the 2013 International Symposium on Code Generation and Optimization (CGO)*, February 2013.
- [39] Arun Raman, Jae W. Lee, and David I. August, “From Sequential Programming to Flexible Parallel Execution,” in *Proceedings of the International Conference on Compilers and Synthesis for Embedded Systems (CASES)*, October 2012. Invited.
- [40] Daniel Schwartz-Narbonne, Feng Liu, David I. August, and Sharad Malik, “PASSERT: A Tool for Debugging Parallel Programs,” in *Proceedings of the 18th International Conference on Computer-Aided Verification (CAV)*, June 2012.
- [41] Arun Raman, Ayal Zaks, Jae W. Lee, and David I. August, “Parcae: A System for Flexible Parallel Execution,” in *Proceedings of the 33rd ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, June 2012.
- [42] Nick P. Johnson, Hanjun Kim, Prakash Prabhu, Ayal Zaks, and David I. August, “Speculative Separation for Privatization and Reductions,” in *Proceedings of the 33rd ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, June 2012.
- [43] Yun Zhang, Soumyadeep Ghosh, Jialu Huang, Jae W. Lee, Scott A. Mahlke, and David I. August, “Runtime Asynchronous Fault Tolerance via Speculation,” in *Proceedings of the 2012 International Symposium on Code Generation and Optimization (CGO)*, April 2012.
- [44] Hanjun Kim, Nick P. Johnson, Jae W. Lee, Scott A. Mahlke, and David I. August, “Automatic Speculative DOALL for Clusters,” in *Proceedings of the 2012 International Symposium on Code Generation and Optimization (CGO)*, March 2012.
- [45] Thomas B. Jablin, James A. Jablin, Prakash Prabhu, Feng Liu, and David I. August, “Dynamically Managed Data for CPU-GPU Architectures,” in *Proceedings of the 2012 International Symposium on Code Generation and Optimization (CGO)*, March 2012.
- [46] Kangkook Jee, Georgios Portokalidis, Vasileios P. Kemerlis, Soumyadeep Ghosh, David I. August, and Angelos D. Keromytis, “A General Approach for Efficiently Accelerating Software-based Dynamic Data Flow Tracking on Commodity Hardware,” in *Proceedings of the 19th Internet Society (ISOC) Symposium on Network and Distributed Systems Security (NDSS)*, February 2012.
- [47] Shantanu Gupta, Shuguang Feng, Amin Ansari, Scott A. Mahlke, and David I. August, “Bundled Execution of Recurring Traces for Energy-Efficient General Purpose Processing,” in *Proceedings of the 44th IEEE/ACM International Symposium on Microarchitecture (MICRO)*, December 2011.  
**One of six papers nominated for the Best Paper Award by the Program Committee.**
- [48] Shuguang Feng, Shantanu Gupta, Amin Ansari, Scott A. Mahlke, and David I. August, “Low-cost, Fine-grained Transient Fault Recovery for Low-end Commodity Systems,” in *Proceedings of the 44th IEEE/ACM International Symposium on Microarchitecture (MICRO)*, December 2011.

- [49] Prakash Prabhu, Thomas B. Jablin, Arun Raman, Yun Zhang, Jialu Huang, Hanjun Kim, Nick P. Johnson, Feng Liu, Soumyadeep Ghosh, Stephen Beard, Taewook Oh, Matthew Zoufaly, David Walker, and David I. August, “A Survey of the Practice of Computational Science,” in *Proceedings of the 24th ACM/IEEE Conference on High Performance Computing, Networking, Storage and Analysis (SC)*, November 2011.
- [50] Daniel Schwartz-Narbonne, Feng Liu, Tarun Pondicherry, David I. August, and Sharad Malik, “Parallel Assertions for Debugging Parallel Programs,” in *2011 9th IEEE/ACM International Conference on Formal Methods and Models for Codesign (MEMOCODE)*, July 2011.
- [51] Prakash Prabhu, Soumyadeep Ghosh, Yun Zhang, Nick P. Johnson, and David I. August, “Commutative Set: A Language Extension for Implicit Parallel Programming,” in *Proceedings of the 32nd ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, June 2011.
- [52] Thomas B. Jablin, Prakash Prabhu, James A. Jablin, Nick P. Johnson, Stephen R. Beard, and David I. August, “Automatic CPU-GPU Communication Management and Optimization,” in *Proceedings of the 32nd ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, June 2011.
- [53] Arun Raman, Hanjun Kim, Taewook Oh, Jae W. Lee, and David I. August, “Parallelism Orchestration using DoPE: the Degree of Parallelism Executive,” in *Proceedings of the 32nd ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, June 2011.
- [54] Hanjun Kim, Arun Raman, Feng Liu, Jae W. Lee, and David I. August, “Scalable Speculative Parallelization on Commodity Clusters,” in *Proceedings of the 43rd IEEE/ACM International Symposium on Microarchitecture (MICRO)*, December 2010.  
**Highest ranked paper in double-blind review process.**
- [55] Yun Zhang, Jae W. Lee, Nick P. Johnson, and David I. August, “DAFT: Decoupled Acyclic Fault Tolerance,” in *Proceedings of the 19th International Conference on Parallel Architectures and Compilation Techniques (PACT)*, September 2010.  
**Selected by the Program Committee as a “top paper” for inclusion in a special issue of the International Journal of Parallel Programming (IJPP).**
- [56] Jialu Huang, Arun Raman, Yun Zhang, Thomas B. Jablin, Tzu-Han Hung, and David I. August, “Decoupled Software Pipelining Creates Parallelization Opportunities,” in *Proceedings of the 2010 International Symposium on Code Generation and Optimization (CGO)*, April 2010.
- [57] Arun Raman, Hanjun Kim, Thomas R. Mason, Thomas B. Jablin, and David I. August, “Speculative Parallelization Using Software Multi-threaded Transactions,” in *Proceedings of the Fifteenth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March 2010.
- [58] Easwaran Raman, Guilherme Ottoni, Arun Raman, Matthew Bridges, and David I. August, “Parallel-Stage Decoupled Software Pipelining,” in *Proceedings of the 2008 International Symposium on Code Generation and Optimization (CGO)*, April 2008.
- [59] Easwaran Raman, Neil Vachharajani, Ram Rangan, and David I. August, “Spice: Speculative Parallel Iteration Chunk Execution,” in *Proceedings of the 2008 International Symposium on Code Generation and Optimization (CGO)*, April 2008.
- [60] Guilherme Ottoni and David I. August, “Communication Optimizations for Global Multi-Threaded Instruction Scheduling,” in *Proceedings of the 13th ACM International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March 2008.
- [61] Guilherme Ottoni and David I. August, “Global Multi-Threaded Instruction Scheduling,” in *Proceedings of the 40th IEEE/ACM International Symposium on Microarchitecture (MICRO)*, December 2007.
- [62] Matthew J. Bridges, Neil Vachharajani, Yun Zhang, Thomas B. Jablin, and David I. August, “Revisiting the Sequential Programming Model for Multi-Core,” in *Proceedings of the 40th IEEE/ACM International Symposium on Microarchitecture (MICRO)*, December 2007.  
**Selected for IEEE Micro’s “Top Picks” special issue for papers “most relevant to industry and significant in contribution to the field of computer architecture” in 2007.**

- [63] Neil Vachharajani, Ram Rangan, Easwaran Raman, Matthew J. Bridges, Guilherme Ottoni, and David I. August, "Speculative Decoupled Software Pipelining," in *Proceedings of the 16th International Conference on Parallel Architectures and Compilation Techniques (PACT)*, September 2007.
- [64] Frances Perry, Lester Mackey, George A. Reis, Jay Ligatti, David I. August, and David Walker, "Fault-tolerant Typed Assembly Language," in *Proceedings of the 2007 ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, June 2007.  
**Winner Best Paper Award.**
- [65] Bolei Guo, Neil Vachharajani, and David I. August, "Shape Analysis with Inductive Recursion Synthesis," in *Proceedings of the ACM SIGPLAN 2007 Conference on Programming Language Design and Implementation (PLDI)*, June 2007.
- [66] Ram Rangan, Neil Vachharajani, Adam Stoler, Guilherme Ottoni, David I. August, and George Z. N. Cai, "Support for High-Frequency Streaming in CMPs," in *Proceedings of the 39th IEEE/ACM International Symposium on Microarchitecture (MICRO)*, December 2006.
- [67] David Walker, Lester Mackey, Jay Ligatti, George A. Reis, and David I. August, "Static Typing for a Faulty Lambda Calculus," in *Proceedings of the 11th ACM SIGPLAN International Conference on Functional Programming (ICFP)*, September 2006.
- [68] Jonathan Chang, George A. Reis, and David I. August, "Automatic Instruction-Level Software-Only Recovery," in *Proceedings of the International Conference on Dependable Systems and Networks (DSN)*, June 2006.  
**Winner of the William C. Carter Award.**  
**Selected for IEEE Micro's "Top Picks" special issue for papers "most relevant to industry and significant in contribution to the field of computer architecture" in 2006.**
- [69] Matthew J. Bridges, Neil Vachharajani, Guilherme Ottoni, and David I. August, "Automatic Instruction Scheduler Retargeting by Reverse-Engineering," in *Proceedings of the 2006 ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, June 2006.
- [70] Spyridon Triantafyllis, Matthew J. Bridges, Easwaran Raman, Guilherme Ottoni, and David I. August, "A Framework for Unrestricted Whole-Program Optimization," in *Proceedings of the 2006 ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, June 2006.
- [71] Bolei Guo, Youfeng Wu, Cheng Wang, Matthew J. Bridges, Guilherme Ottoni, Neil Vachharajani, Jonathan Chang, and David I. August, "Selective Runtime Memory Disambiguation in a Dynamic Binary Translator," in *Proceedings of the 15th International Conference on Compiler Construction (CC)*, March 2006.
- [72] David A. Penry, Daniel Fay, David Hodgdon, Ryan Wells, Graham Schelle, David I. August, and Daniel A. Connors, "Exploiting Parallelism and Structure to Accelerate the Simulation of Chip Multiprocessors," in *Proceedings of the Twelfth International Symposium on High-Performance Computer Architecture (HPCA)*, February 2006.
- [73] Guilherme Ottoni, Ram Rangan, Adam Stoler, and David I. August, "Automatic Thread Extraction with Decoupled Software Pipelining," in *Proceedings of the 38th IEEE/ACM International Symposium on Microarchitecture (MICRO)*, November 2005.  
**One of five papers nominated for the Best Paper Award by the Program Committee.**
- [74] Guilherme Ottoni, Ram Rangan, Adam Stoler, and David I. August, "A New Approach to Thread Extraction for General-Purpose Programs," in *Proceedings of the 2nd Watson Conference on Interaction between Architecture, Circuits, and Compilers (PAC2)*, September 2005.
- [75] George A. Reis, Jonathan Chang, Neil Vachharajani, Ram Rangan, David I. August, and Shubhendu S. Mukherjee, "Design and Evaluation of Hybrid Fault-Detection Systems," in *Proceedings of the 32nd International Symposium on Computer Architecture (ISCA)*, June 2005.
- [76] Bolei Guo, Matthew J. Bridges, Spyridon Triantafyllis, Guilherme Ottoni, Easwaran Raman, and David I. August, "Practical and Accurate Low-Level Pointer Analysis," in *Proceedings of the Third International Symposium on Code Generation and Optimization (CGO)*, March 2005.

- [77] George A. Reis, Jonathan Chang, Neil Vachharajani, Ram Rangan, and David I. August, “SWIFT: Software Implemented Fault Tolerance,” in *Proceedings of the Third International Symposium on Code Generation and Optimization (CGO)*, March 2005.  
**Winner Best Paper Award.**  
**Winner of the 2015 International Symposium on Code Generation and Optimization Test of Time Award.**
- [78] Neil Vachharajani, Matthew J. Bridges, Jonathan Chang, Ram Rangan, Guilherme Ottoni, Jason A. Blome, George A. Reis, Manish Vachharajani, and David I. August, “RIFLE: An Architectural Framework for User-Centric Information-Flow Security,” in *Proceedings of the 37th International Symposium on Microarchitecture (MICRO)*, December 2004.
- [79] Loukas Georgiadis, Renato F. Werneck, Robert E. Tarjan, Spyridon Triantafyllis, and David I. August, “Finding Dominators in Practice,” in *Proceedings of the 12th European Symposium on Algorithms*, September 2004.
- [80] Manish Vachharajani, Neil Vachharajani, Sharad Malik, and David I. August, “Facilitating Reuse in Hardware Models with Enhanced Type Inference,” in *The IEEE/ACM/IFIP Second International Conference on Hardware/Software Codesign and System Synthesis (ISSS)*, September 2004.
- [81] Ram Rangan, Neil Vachharajani, Manish Vachharajani, and David I. August, “Decoupled Software Pipelining with the Synchronization Array,” in *Proceedings of the 13th International Conference on Parallel Architectures and Compilation Techniques (PACT)*, September 2004.  
**Highest ranked paper in double-blind review process.**
- [82] Manish Vachharajani, Neil Vachharajani, and David I. August, “The Liberty Structural Specification Language: A High-Level Modeling Language for Component Reuse,” in *Proceedings of the 2004 ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, June 2004.
- [83] Qiang Wu, Artem Pyatakov, Alexey N. Spiridonov, Easwaran Raman, Douglas W. Clark, and David I. August, “Exposing Memory Access Regularities Using Object-Relative Memory Profiling,” in *Proceedings of the Second International Symposium on Code Generation and Optimization (CGO)*, March 2004.
- [84] David A. Penry and David I. August, “Optimizations for a Simulator Construction System Supporting Reusable Components,” in *Proceedings of the 40th Design Automation Conference (DAC)*, June 2003.
- [85] Spyridon Triantafyllis, Manish Vachharajani, Neil Vachharajani, and David I. August, “Compiler Optimization-Space Exploration,” in *Proceedings of the 2003 International Symposium on Code Generation and Optimization (CGO)*, March 2003.  
**Winner Best Paper Award.**
- [86] Manish Vachharajani, Neil Vachharajani, David A. Penry, Jason A. Blome, and David I. August, “Microarchitectural Exploration with Liberty,” in *Proceedings of the 35th International Symposium on Microarchitecture (MICRO)*, November 2002.  
**Winner Best Student Paper Award.**
- [87] Kaiyu Chen, Sharad Malik, and David I. August, “Retargetable Static Timing Analysis for Embedded Software,” in *Proceedings of the 14th International Symposium on System Synthesis (ISSS)*, October 2001.
- [88] John W. Sias, Wen-mei W. Hwu, and David I. August, “Accurate and Efficient Predicate Analysis with Binary Decision Diagrams,” in *Proceedings of the 33rd International Symposium on Microarchitecture (MICRO)*, December 2000.
- [89] Daniel A. Connors, Jean-Michel Puiatti, David I. August, Kevin M. Crozier, and Wen-mei W. Hwu, “An Architecture Framework for Introducing Predicated Execution into Embedded Microprocessors,” in *Proceedings of the Fifth European Conference on Parallel Processing (EUROPAR)*, September 1999.
- [90] David I. August, John W. Sias, Jean-Michel Puiatti, Scott A. Mahlke, Daniel A. Connors, Kevin M. Crozier, and Wen-mei W. Hwu, “The Program Decision Logic Approach to Predicated Execution,” in *Proceedings of the 26th International Symposium on Computer Architecture (ISCA)*, May 1999.



- [91] David I. August, Daniel A. Connors, Scott A. Mahlke, John W. Sias, Kevin M. Crozier, Ben-Chung Cheng, Patrick R. Eaton, Qudus B. Olaniran, and Wen-mei W. Hwu, “Integrated Predicated and Speculative Execution in the IMPACT EPIC Architecture,” in *Proceedings of the 25th International Symposium on Computer Architecture (ISCA)*, July 1998.
- [92] David I. August, Wen-mei W. Hwu, and Scott A. Mahlke, “A Framework for Balancing Control Flow and Predication,” in *Proceedings of the 30th International Symposium on Microarchitecture (MICRO)*, December 1997.  
**Selected as an “outstanding paper” for inclusion in a special issue of the International Journal of Parallel Programming (IJPP) by the Program Committee.**
- [93] David I. August, Daniel A. Connors, John C. Gyllenhaal, and Wen-mei W. Hwu, “Architectural Support Compiler-Synthesized Dynamic Branch Prediction Strategies: Rationale and Initial Results,” in *Proceedings of the Third International Symposium on High-Performance Computer Architecture (HPCA)*, February 1997.
- [94] Scott A. Mahlke, Rick E. Hank, James E. McCormick, David I. August, and Wen-mei W. Hwu, “A Comparison of Full and Partial Predicated Execution Support for ILP Processors,” in *Proceedings of the 22nd International Symposium on Computer Architecture (ISCA)*, June 1995.

#### REFEREED WORKSHOP PUBLICATIONS

- [95] Zujun Tan, Greg Chan, Ziyang Xu, Sotiris Apostolakis, and David I. August, “Automatic and Speculative Parallel-Stage Decoupled Software Pipelining,” in *The Second Young Architect Workshop (YArch)*, March 2020.
- [96] Ziyang Xu, Greg Chan, Sotiris Apostolakis, and David I. August, “Collaborative Parallelization Framework,” in *The First Young Architect Workshop (YArch)*, February 2019.
- [97] Simha Sethumadhavan, Salvatore J. Stolfo, Angelos D. Keromytis, Junfeng Yang, and David I. August, “The SPARCHS Project: Hardware Support for Software Security,” in *Proceedings of the First SysSec Workshop (SYSSEC)*, July 2011.
- [98] Thomas B. Jablin, Yun Zhang, James A. Jablin, Jialu Huang, Hanjun Kim, and David I. August, “Liberty Queues for EPIC Architectures,” in *Proceedings of the Eighth Workshop on Explicitly Parallel Instruction Computer Architectures and Compiler Technology (EPIC)*, April 2010.
- [99] Guilherme Ottoni and David I. August, “Global Multi-Threaded Instruction Scheduling: Technique and Initial Results,” in *Proceedings of the Sixth Workshop on Explicitly Parallel Instruction Computer Architectures and Compiler Technology (EPIC)*, March 2007.
- [100] Jonathan Chang, George A. Reis, and David I. August, “Non-Uniform Fault Tolerance,” in *Proceedings of the 2nd Workshop on Architectural Reliability (WAR)*, December 2006.
- [101] George A. Reis, Jonathan Chang, David I. August, Robert Cohn, and Shubhendu S. Mukherjee, “Configurable Transient Fault Detection via Dynamic Binary Translation,” in *Proceedings of the 2nd Workshop on Architectural Reliability (WAR)*, December 2006.
- [102] Ram Rangan and David I. August, “Amortizing Software Queue Overhead for Pipelined Inter-Thread Communication,” in *Proceedings of the Workshop on Programming Models for Ubiquitous Parallelism (PMUP)*, September 2006.
- [103] George A. Reis, David I. August, Robert Cohn, and Shubhendu S. Mukherjee, “Software Fault Detection Using Dynamic Instrumentation,” in *Proceedings of the Fourth Annual Boston Area Architecture Workshop (BARC)*, February 2006.
- [104] Neil Vachharajani, Matthew Iyer, Chinmay Ashok, Manish Vachharajani, David I. August, and Daniel A. Connors, “Chip Multi-Processor Scalability for Single-Threaded Applications,” in *Proceedings of the 2005 Workshop on Design, Architecture and Simulation of Chip Multi-Processors (dasCMP)*, November 2005.

- [105] David A. Penry, Manish Vachharajani, and David I. August, “Rapid Development of Flexible Validated Processor Models,” in *Proceedings of the Workshop on Modeling, Benchmarking, and Simulation (MoBS)*, June 2005.
- [106] Easwaran Raman and David I. August, “Recursive Data Structure Profiling,” in *Proceedings of the Third Annual ACM SIGPLAN Workshop on Memory Systems Performance (MSP)*, June 2005.
- [107] Guilherme Ottoni, Ram Rangan, Neil Vachharajani, and David I. August, “Decoupled Software Pipelining: A Promising Technique to Exploit Thread-Level Parallelism,” in *Proceedings of the Fourth Workshop on Explicitly Parallel Instruction Computer Architectures and Compiler Technology (EPIC)*, March 2005.
- [108] Jason Blome, Manish Vachharajani, Neil Vachharajani, and David I. August, “The Liberty Simulation Environment as a Pedagogical Tool,” in *Proceedings of the Workshop on Computer Architecture Education (WCAE)*, June 2003.
- [109] Spyridon Triantafyllis, Manish Vachharajani, and David I. August, “Procedure Boundary Elimination for EPIC Compilers,” in *Proceedings of the Second Workshop on Explicitly Parallel Instruction Computer Architectures and Compiler Technology (EPIC)*, November 2002.
- [110] Wei Qin, Subramanian Rajagopalan, Manish Vachharajani, Hangsheng Wang, Xinpeng Zhu, David I. August, Kurt Keutzer, Sharad Malik, and Li-Shiuan Peh, “Design Tools for Application Specific Embedded Processors,” in *Proceedings of the Second International Workshop on Embedded Software, Lecture Notes in Computer Science (EMSOFT)*, October 2002. Invited.
- [111] David I. August, Kurt Keutzer, Sharad Malik, and A. Richard Newton, “A Disciplined Approach to the Development of Platform Architectures,” in *Proceedings of the Tenth Workshop on Synthesis and System Integration of Mixed Technologies (SASIMI)*, April 2001. Invited.

#### TECHNICAL REPORTS

- [112] David A. Penry, Manish Vachharajani, and David I. August, “Rapid Development of Flexible Validated Processor Models,” *Liberty Research Group Technical Report 04-03*, November 2004.
- [113] Manish Vachharajani, Neil Vachharajani, David A. Penry, Jason A. Blome, Sharad Malik, and David I. August, “The Liberty Simulation Environment: A Deliberate Approach to High-Level System Modeling,” *Liberty Research Group Technical Report 04-02*, March 2004.
- [114] Manish Vachharajani and David I. August, “A Study of the Clarity of Functionally and Structurally Composed High-level Simulation Models,” *Liberty Research Group Technical Report 04-01*, January 2004.
- [115] Manish Vachharajani, Neil Vachharajani, and David I. August, “A Comparison of Reuse in Object-oriented Programming and Structural Modeling Systems,” *Liberty Research Group Technical Report 03-01*, October 2003.
- [116] David I. August, Daniel A. Connors, John W. Sias, Kevin M. Crozier, Patrick R. Eaton, Qudus B. Olaniran, and Wen-mei W. Hwu, “The IMPACT EPIC 1.0 Architecture and Instruction Set Reference Manual,” *University of Illinois at Urbana/Champaign Center for Reliable and High Performance Computing Technical Report CRHC-98-04*, February 1998.
- [117] David I. August, Brian L. Deitrich, and Scott A. Mahlke, “Sentinel Scheduling with Recovery Blocks,” *University of Illinois at Urbana/Champaign Center for Reliable and High Performance Computing Technical Report CRHC-95-05*, February 1995.

## OTHER PUBLICATIONS

- [118] Mojtaba Mehrara, Thomas B. Jablin, Dan Upton, David I. August, Kim Hazelwood, and Scott Mahlke, “Compilation Strategies and Challenges for Multicore Signal Processing,” in *IEEE Signal Processing Magazine*, November 2009.
- [119] David I. August, Kurt Keutzer, Sharad Malik, and Richard Newton, “Programmable ASICs to Reduce Costs,” in *EE Times*, November 2000.
- [120] David I. August, “Systematic Compilation for Predicated Execution,” Ph.D. Dissertation, University of Illinois at Urbana-Champaign, May 2000.

## RELEASED SOFTWARE

- [121] Sotiris Apostolakis, Ziyang Xu, Zujun Tan, Greg Chan, Simone Campanoni, and David I. August, “Perspective: A Sensible Approach to Speculative Automatic Parallelization,” Released in December 2020, available at <https://liberty.princeton.edu/Projects/AutoPar/Perspective/>.
- [122] Sotiris Apostolakis, Ziyang Xu, Zujun Tan, David I. August, and Simone Campanoni, “NOELLE Offers Empowering LLVM Extensions,” Released in December 2020, available at <https://liberty.princeton.edu/Projects/NOELLE/>.
- [123] Sotiris Apostolakis, Ziyang Xu, Zujun Tan, Greg Chan, Simone Campanoni, and David I. August, “SCAF: A Speculation-Aware Collaborative Dependence Analysis Framework,” Released in December 2020, available at <https://liberty.princeton.edu/Projects/AutoPar/SCAF/>.
- [124] Manish Vachharajani, David A. Penry, Neil Vachharajani, Jason A. Blome, and David I. August, “Liberty Simulation Environment, Version 1.0,” Released in December 2003, available at <http://liberty.princeton.edu/Software/LSE>.

## PATENTS

- [125] David I. August, Soumyadeep Ghosh, and Jordan Fix, “Trust Architecture and Related Methods,” United States Patent Number 10,599,853, March 2020.
- [126] David I. August, Kevin C. Fan, Jae Wook Lee, Scott A. Mahlke, and Mojtaba Mehrara, “Cooperative Program Code Transformation,” United States Patent Number 9,329,846, May 2016.
- [127] David I. August, Neil Vachharajani, and Matthew J. Bridges, “System and Method for Supporting Multi-Threaded Transactions,” United States Patent Number 9,128,750, September 2015.
- [128] Wen-mei W. Hwu, Daniel A. Connors, David I. August, and John W. Sias, “Method and Apparatus for Enhancing Instruction Level Parallelism,” United States Patent Number 6,640,315, October 2003.