

# David I. August

## Curriculum Vitae

### CONTACT INFORMATION

Department of Computer Science  
Princeton University  
35 Olden Street  
Princeton, NJ 08540

Phone: (609) 258-2085  
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august@princeton.edu  
<http://august.princeton.edu>

### EDUCATION

*University of Illinois at Urbana-Champaign, Urbana, IL*

Ph.D. in Electrical and Computer Engineering, May 2000

Thesis: "Systematic Compilation for Predicated Execution," Advisor: Wen-mei W. Hwu

M.S. in Electrical and Computer Engineering, May 1996

Advisor: Wen-mei W. Hwu

*Rensselaer Polytechnic Institute, Troy, NY*

B.S. in Electrical Engineering, Summa Cum Laude (1/1249), May 1993

### EXPERIENCE

**Professor**, July 2012 to Present; **Associate Professor**, July 2006 to June 2012; **Assistant Professor**, February 2000 to June 2006; **Lecturer**, August 1999 to January 2000  
*Department of Computer Science, Princeton University, Princeton, NJ*

**Consultant**, August 1998-Present

*Technology and intellectual property consulting*

**Research Intern**, May to September 1996, November 1996

*Intel Corporation, Santa Clara, CA*

**Research Intern**, May to August 1995

*Hewlett Packard Laboratories, Santa Clara, CA*

**Architecture Validation Engineer**, May to August 1994

*Intel Corporation, Hillsboro, OR*

### RECOGNITION

- Elevation to IEEE Fellow "for contributions to compilers and architectures for multicore and parallel processing systems".
- Selection of "SWIFT: Software Implemented Fault Tolerance," for "The Test of Time Award" at The Thirteenth International Symposium on Code Generation and Optimization (CGO), 2015.
- Selection of "DAFT: Decoupled Acyclic Fault Tolerance" by the program committee for inclusion in special issue of *The International Journal of Parallel Processing* composed of "top papers" from the 19th International Conference on Parallel Architectures and Compilation Techniques (PACT), 2010.
- Nomination of "Fault-tolerant Typed Assembly Language" as a Communications of the ACM (CACM) Research Highlight, September 2008.
- Selection of "Revisiting the Sequential Programming Model for Multi-Core" for IEEE Micro's "Top Picks" special issue for papers "most relevant to industry and significant in contribution to the field of computer architecture" in 2007.
- Best Paper Award for "Fault-tolerant Typed Assembly Language" at the 2007 ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI), June 2007.
- Selection of "Automatic Instruction-Level Software-Only Recovery Methods" for IEEE Micro's "Top Picks" special issue for papers "most relevant to industry and significant in contribution to the field of computer architecture" in 2006.
- Selection of "Automatic Instruction-Level Software-Only Recovery Methods" for the William C. Carter Award at the International Conference on Dependable Systems and Networks, June 2006.

- Best Paper Award for “SWIFT: Software Implemented Fault Tolerance” at the Third Annual ACM/IEEE International Symposium on Code Generation and Optimization (CGO), March 2005.
- Emerson Electric Company E. Lawrence Keyes ’51 Faculty Advancement Award, June 2003.
- Dean’s letter of recognition for teaching, Spring 2003.
- Best Paper Award for “Compiler Optimization-Space Exploration” at the First Annual ACM/IEEE International Symposium on Code Generation and Optimization (CGO), March 2003.
- Best Student Paper Award for “Microarchitectural Exploration with Liberty” at the 35th Annual ACM/IEEE International Symposium on Microarchitecture (MICRO), November 2002.
- National Science Foundation Faculty Early Career Development Award (CAREER), 2002.
- Invited presentation at University of Virginia, *Top Gun Lecture Series* recognizing “faculty on a trajectory to be research leaders of the coming decades,” December 2001.
- IBM Faculty Partnership Award, 2001-2002.
- Princeton University Research Board Award, 2001-2002.
- One of five featured by *The Chronicle of Higher Education* in its annual list of “New Ph.D.’s to Watch,” September 1999.
- Selection of “A Framework for Balancing Control Flow and Predication” by the program committee for inclusion in special issue of *The International Journal of Parallel Processing* composed of “outstanding papers” from the 30th Annual ACM/IEEE International Symposium on Microarchitecture (MICRO), 1999.
- Intel Foundation Graduate Fellowship, 1996-1997.
- Department of Defense, Office of Naval Research Graduate Fellowship, 1993-1996.
- University of Illinois Henry O. Koehler Graduate Fellowship, 1993-1994.

## ACTIVITIES

### PROGRAM CHAIR

- The 42nd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO) (with José Martínez, Cornell), 2009.
- The Fifth Annual International Symposium on Code Generation and Optimization (CGO) (with Chris J. Newburn, Intel), 2007.
- The IEEE International Conference on Computer Design (ICCD) - Computer Systems Design and Applications Track (with Mark Charney, Intel), 2003.
- The IEEE International Conference on Computer Design (ICCD) - Computer Systems Design and Applications Track (with Mark Charney, Intel), 2002.

### EDITING

- Guest Editor, IEEE Micro, special issue on “Parallelization of Sequential Code,” July 2012.
- Editorial Board, IEEE Computer Architecture Letters, 2010 - 2014.
- Associate Editor, ACM Transactions on Architecture and Code Optimization, 2006 - present.
- Guest Editor, Computer Languages, Systems and Structures special issue on “Programming Language and Compiler Support for Secure and Reliable Computing,” April 2006.

### TECHNICAL PROGRAM COMMITTEES

- The CGO 2007 Test of Time Award Selection Committee, 2017
- The 22nd International Conference on Compiler Construction (CC), 2015
- The 41st Annual IEEE/ACM International Symposium on Computer Architecture (ISCA), 2014.
- IEEE MICRO Top-Picks in Computer Architecture, 2013.
- The ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI), 2013.
- IEEE MICRO Top-Picks in Computer Architecture, 2011.
- The Fourth Workshop on Parallel Execution of Sequential Programs on Multi-core Architectures (PE-SPMA), 2011
- The 11th International Symposium on Advanced Parallel Processing Technologies (APPT), 2011
- The First International Workshop on Future Architectural Support for Parallel Programming (FASPP), 2011
- The 16th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2011.

- The 43rd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), 2010.
- The Third Workshop on Emerging Applications and Many-core Architecture (EAMA), 2010.
- The Sixth Workshop on Modeling, Benchmarking and Simulation (MoBS), 2010.
- The First Workshop on Accelerators for High-performance Architectures (WAHA), 2009
- The Fifth IEEE International Symposium on Workload Characterization (IISWC), 2009.
- The ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI), 2008.
- IEEE MICRO Top-Picks in Computer Architecture, 2007.
- The Sixth Annual Workshop on Duplicating, Deconstructing, and Debunking (WDDD), 2007.
- The ACM International Conference on Computing Frontiers (CF), 2007.
- The 34th Annual IEEE/ACM International Symposium on Computer Architecture (ISCA), 2007.
- The 39th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), 2006.
- The International Conference on High Performance Embedded Architectures and Compilers (HiPEAC), 2006.
- The Workshop on Introspective Architectures (WISA), 2006.
- The 15th International Conference on Parallel Architectures and Compilation Techniques (PACT), 2006.
- The Second Workshop on Modeling, Benchmarking and Simulation (MoBS), 2006.
- The 10th Workshop on Interaction between Compilers and Computer Architectures (INTERACT), 2006.
- The IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2006.
- The 32nd Annual IEEE/ACM International Symposium on Computer Architecture (ISCA), 2005.
- The Workshop on Modeling, Benchmarking and Simulation (MoBS), 2005.
- The IEEE/ACM International Conference on Computer Aided Design (ICCAD), 2005.
- The International Conference on High Performance Embedded Architectures and Compilers (HiPEAC), 2005.
- The Third Annual International Symposium on Code Generation and Optimization (CGO), 2005.
- The International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), 2004.
- The IEEE International Conference on Computer Design (ICCD) - Computer Systems Design and Applications Track, 2004.
- The IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2004.
- The Second Annual International Symposium on Code Generation and Optimization (CGO), 2004.
- The 30th Annual IEEE/ACM International Symposium on Computer Architecture (ISCA), 2003.
- The First Annual International Symposium on Code Generation and Optimization (CGO), 2003.
- The IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2003.
- The 35th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), 2002.
- The ACM Workshop on Languages, Compilers, and Tools for Embedded Systems (LCTES), 2002.
- The ACM International Conference on Measurement and Modeling of Computer Systems (SIGMETRICS), 2002.
- The 6th Workshop on Interaction between Compilers and Computer Architectures (INTERACT), 2002.
- The First Annual Workshop on Explicitly Parallel Instruction Computer Architectures and Compiler Technology (EPIC), 2001.
- The ACM Workshop on Languages, Compilers, and Tools for Embedded Systems (LCTES), 2001.
- The IEEE International Conference on Computer Design (ICCD), 2001.
- The 7th International IEEE Symposium on High-Performance Computer Architecture (HPCA), 2000.
- The IEEE International Conference on Computer Design (ICCD), 2000.

#### CONFERENCE ORGANIZING AND STEERING COMMITTEES

- Steering Committee, The International Symposium on Code Generation and Optimization (CGO), 2007-2010.
- General Chair, The Fourth Annual International Symposium on Code Generation and Optimization (CGO), 2006.
- Publications Chair, The IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2003.
- Finance Chair, The Second Annual International Symposium on Code Generation and Optimization (CGO), 2003
- General Chair, The Second Annual Workshop on Explicitly Parallel Instruction Computer Architectures and Compiler Technology (EPIC), 2002.

## TECHNICAL PANELS

- Panelist, “Advancing Computer Systems without Technology Progress,” DARPA Information Science and Technology (ISAT) Workshop, March 2012.
- Panelist, “Freedom from the Tyranny of Parallel Programming,” Workshop on Deterministic Multiprocessing and Parallel Programming (WoDet), November 2009.
- Panelist, “Programming for Multi-core Processors (OR NOT?)” Second Workshop on Computer Architecture Research Directions (CARD) held in conjunction with International Symposium on Computer Architecture (ISCA), June 2009.
- Panelist, “Are New Programming Languages Needed to Exploit Manycore Architectures?” Microsoft Research Faculty Summit, July 2007.
- Panelist, “Programming Languages/Models and Compiler Technologies,” Manycore Computing Workshop held in conjunction with the International Conference on Supercomputing (ICS), June 2007.
- Panelist, “Are New Languages Necessary for Multicore,” The Fifth International Symposium on Code Generation and Optimization (CGO), March 2007.
- Panelist, “Directions in Multi-Core Research,” Microsoft Corporation, Redmond, WA, January 2007.
- Panelist, “What should architects know about compilers and systems software?” The Computing Research Association’s Committee on the Status of Women (CRA-W) and the Coalition to Diversify Computing (CDC) Computer Architecture Summer School, 2006.
- Panelist, “Design Methodologies for Future Processor Chips,” The Second Workshop on Modeling, Benchmarking and Simulation held in conjunction with the 33rd International Symposium on Computer Architecture (ISCA), 2006.
- Panelist, “Simulation Methodology,” Third Annual Workshop on Duplicating, Deconstructing, and Debunking (WDDD) held in conjunction with International Symposium on Computer Architecture (ISCA), 2004.
- Panelist, “Emerging Issues with Simulation Technology” NSF-Sponsored Workshop, Austin, TX, December 2001.

## FUNDING PANELS

- National Science Foundation Secure and Trusted Cyberspace Panel (SaTC)
- National Science Foundation Software and Hardware Foundations Panel (SHF)
- National Science Foundation Computing Systems Research Panel (CSR) (2 times)
- National Science Foundation Computer Systems Architecture Panel (CSA)
- National Science Foundation Information Technology Research Panel (ITR)
- National Science Foundation Next Generation Software Panel (NGS)

## TUTORIALS

- “Next Generation Automatic Parallelization,” presented at the Eighth International Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems, Fiuggi, Italy, June 2012.
- “Fault Tolerant Computing,” Summer School on Language-Based Techniques for Integrating with the External World, July 2007.
- “Structural Simulation,” presented at the First International Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems, L’Aquila, Italy, June 2005.
- “Using The Liberty Simulation Environment with emphasis on validated OS-level simulation,” presented at the 11th International Conference on Architectural Support for Programming Languages and Operating Systems in Boston, MA, October 2004.
- “The Liberty Simulation Environment, Version 1.0,” presented at the 36th International Symposium on Microarchitecture in San Diego, CA, December 2003.
- “Architectural Exploration with Liberty,” presented at the International Symposium on Microarchitecture in Austin, TX, December 2001.
- “Future Technologies and Markets for Programmable Platform-Based Design,” presented at IP/SoC 2001 in Santa Clara, CA, March 2001.

## INVITED TALKS

- Keynote: “Thoughts on Restoring Computing’s Former Glory,” presented at the 2012 Compiler, Archi-

ecture and Tools Day, Haifa, Israel, November 2012.

- Keynote: “Restoring Computing’s Former Glory,” presented at the 2012 Architecture of Computing Systems Conference, Munich, Germany, March 2012.
- “A Roadmap to Restoring Computing’s Former Glory,” presented at the HiPEAC Industrial Workshop, High-Performance and Embedded Computing, Charmonix, France, April 2011.
- Keynote: “Indistinguishable from Magic,” presented at the 16th Workshop on Compiler Techniques for High-Performance and Embedded Computing, Taipei, Taiwan, May 2010.
- Keynote: “Parallelism for Multicore,” presented at the 2009 Workshop on Parallel Execution of Sequential Programs on Multi-core Architectures held in conjunction with 36th International Symposium on Computer Architecture, June, 2009.
- “Parallelism for Multicore,” presented at the New Jersey Programming Languages Seminar and Princeton Computer Architecture Research Day, March, 2009.
- “Addressing the Multicore Problem,” presented at the Princeton Innovation Forum, March, 2009.
- “Automatic Thread Extraction from Sequential Programs,” presented at Indian Institute of Science, March, 2008.
- “The Multicore Challenge,” DARPA Information Processing Technology Office Futures Panel, December 2007.
- “Automatic Thread Extraction from Sequential Programs,” presented at Microsoft Research Faculty Summit, 2007.
- “Liberating Threads from Sequential Programs,” presented at Purdue University, November 2006.
- “The Jericho Project,” presented at the Workshop on Design, Architecture and Simulation of Chip Multi-Processors, November 2005.
- “Liberating Threads from Sequential Programs,” presented at Intel Microprocessor Laboratories, Hewlett-Packard Laboratories, Sun Microsystems Research Laboratories, INRIA Futurs, Cornell University, Carnegie Mellon University, and Massachusetts Institute of Technology, March-April 2005.
- “Liberating Threads from Sequential Programs,” presented at the New Jersey Programming Languages Seminar, February 2005.
- “Liberty Compiler Research,” presented at IBM T. J. Watson Research Center, April 2004.
- “Liberty Research,” presented at Infineon Corporation and Aachen University, February 2004.
- “Architectural Exploration with Liberty,” presented at the Intel High-Level Design Research Forum, November 2002.
- “Optimization-Space Exploration,” presented at Intel Microprocessor Research Laboratories, Hewlett-Packard Laboratories, and Sun Microsystems Research Laboratories, August 2002.
- “Architectural Exploration with Liberty,” presented at IBM T. J. Watson Research Center, July 2002.
- “Liberty Compiler and Architecture Research,” presented at University of Texas at Austin, April 2002.
- “Architectural Exploration with Liberty,” presented at University of Virginia, *Top Gun Lecture Series* recognizing “faculty on a trajectory to be research leaders of the coming decades,” December 2001.
- “Architectural Exploration with Liberty,” presented at Intel Microprocessor Laboratories, Hewlett-Packard Laboratories, and Sun Microsystems Research Laboratories, May 2001.
- “Architectural Exploration with Liberty,” presented at University of Toronto, Distinguished Lecture Series, May 2001.
- “Systematic Compilation for Predicated Execution,” presented at IBM Tokyo Research Laboratories, Rice University, and University of Illinois at Urbana/Champaign, January-August 2000.
- “Systematic Program Decision Logic Optimization Using Predication,” presented at Intel Microprocessor Research Laboratories, April 1999.
- “Enabling Compiler Technology for Predication,” presented at The Swiss Federal Institute of Technology of Lausanne (École Polytechnique Fédérale de Lausanne), February 1999.
- “Enabling Compiler Technology for Predication,” presented at Compaq Corporation, November 1998.
- “A Global Predication Compilation Framework,” presented at Microsoft Research, November 1998.
- “Predicated Microprocessor Architectures and Their Enabling Compiler Technology,” presented at Silicon Graphics, February 1998.
- “Next Generation Predication Support in the IMPACT Compiler,” presented at The Intel Foundation Fellowship Forum, November 1996.
- “Predicated Execution Architectures: New Research Results and Directions,” presented at The Intel Microprocessor Research Forum, October 1995.

## GRANTS

- “TrustGuard-secured Computing Devices,” The Princeton University Intellectual Property Accelerator Fund, \$100,000, January 2017. (Sole PI)
- “An Architecture for Restoring Trust in Our Personal Computing Systems,” National Science Foundation, Secure and Trustworthy Cyberspace (SaTC) (CNS 1441650), \$500,000, September 2014 to August 2017. (Sole PI)
- “A Framework for Portable Parallel Performance,” National Science Foundation, Exploiting Parallelism and Scalability (XPS) (CCF 1439085), \$300,000, August 2014 to July 2017. (Sole PI)
- “A Platform for Data-Parallel GPU Computing at Princeton,” National Science Foundation, Computing Research Infrastructure (CRI) Program (CNS 1205613), \$350,000, August 2012. (PI with 3 Co-PIs)
- “PRACTICE: Power-Reducing Adaptive Computing Technologies: Intelligent, Cross-layer, and Efficient,” United States Department of Defense (DOD), Defense Advanced Research Projects Agency (DARPA), Power Efficiency Revolution For Embedded Computing Technologies (PERFECT) Program, \$10,928,472, January 2012 to August 2015. (PI with 3 others)
- “A Platform for Data-Parallel GPU Computing at Princeton,” National Science Foundation, Computing Research Infrastructure (CRI) Program (CNS 1205613), \$350,000, August 2012. (PI with 3 Co-PIs)
- “Accelerating the Pace of Research (at Princeton),” Dean for Research Fund, \$50,000, April 2012.
- “Automatic Parallelization for GPUs,” NVIDIA Corporation Academic Partnership Award, \$25,000, December 2010.
- “Accelerating the Pace of Research through Implicitly Parallel Programming,” National Science Foundation, Software Infrastructure for Sustained Innovation Scientific (SI<sup>2</sup>) Software Integration (SSI) Program (OCI 1047879), \$1,740,314, October 2010 to September 2014. (PI with Walker)
- “Greater Philadelphia Innovation Cluster (GPIC) for Energy Efficient Buildings,” United States Energy Regional Innovation Cluster (E-RIC) Initiative, \$3,499,994 (\$129,000,000 overall), October 2010 to September 2015. (Princeton University PI with 4 Co-PIs)
- “SPARCHS: Symbiotic, Polymorphic, Autotomic, Resilient, Clean-Slate, Host Security,” United States Department of Defense (DOD), Defense Advanced Research Projects Agency (DARPA), Clean-slate design of Resilient, Adaptive, Secure Hosts (CRASH) Program, \$6,424,180, September 2010 to September 2014. (PI with 4 others)
- “Scaling the Implicitly Parallel Programming Model with Lifelong Thread Extraction and Dynamic Adaptation,” National Science Foundation, Computer Systems Research (CSR) Program (CNS 0964328), \$1,199,998, May 2010 to April 2013. (PI with Hazelwood and Mahlke)
- “AESOP: Adaptive Environment for Supercompiling with Optimized Parallelism,” United States Department of Defense (DOD), Defense Advanced Research Projects Agency (DARPA), Architecture-Aware Compiler Environment (AACE) Program, \$11,572,332, September 2009 to January 2013. (PI with 4 others)
- “Implicitly Parallel Programming with Dynamic Execution,” LG Electronics, \$40,000, November 2009.
- “Hierarchical Latency and Throughput Optimization of Parallel Applications,” Google Research Award, \$50,000, November 2009.
- “A Hybrid Approach for Petascale Computing: Accelerating Scientific Research ,” National Science Foundation, Small Grants for Exploratory Research (SGER) Program (OCI 0849512), \$102,562, June 2009 to May 2010. (PI with Li and Ostriker)
- “Revisiting the Sequential Programming Model for Multicore Systems,” National Science Foundation, Computing Processes and Artifacts (CPA) Program (CCF 0811580), \$150,000, September 2008 to August 2009. (PI with Hazelwood and Mahlke)
- “Automatically Parallelizing Legacy Binary Code for Multi-Core Architectures via Extraction of Self-Similarity,” United States Department of Defense (DOD), Defense Advanced Research Projects Agency (DARPA), \$300,000, September 2008 to August 2009. (PI with Locasto, Sethumadhavan, and Stolfo)
- “Liberating Threads from Sequential Programs,” Gigascale Silicon Research Center, \$357,000, September 2006 to August 2009. (Sole PI)
- “Well-typed Trustworthy Computing in the Presence of Transient Faults,” National Science Foundation, CyberTrust Program (CNS 0627650), \$1,100,000, September 2006 to June 2010. (Co-PI with Walker, Appel, Clark, and Martonosi)
- “Software-Modulated Fault Tolerance,” National Science Foundation, Computer Systems Research (CSR) Program (CNS 0615250), \$320,000, July 2006 to June 2009. (Sole PI)
- “A Viable Approach to Compiling Sequential Codes for CMPs,” Microsoft Corporation, \$50,000, April

2006.

- “Flow-Based Computer Systems Support for Synergistic Hardware-Software Management of Embedded Systems,” National Science Foundation, Computer Systems Research (CSR) Program (CNS 0509402), \$500,000, September 2005 to August 2009. (Co-PI with Li, Martonosi, and Pe)
- “User-centric Information Flow Security,” Intel Corporation, \$120,000, August 2005 to July 2008.
- “Threading the CMP Needle with Fibers and Frays,” The Microelectronics Advanced Research Corporation (MARCO), \$122,500, April 2005 to August 2006. (Sole PI)
- “International Modular Simulation Research,” Direction des Relations Européennes et Internationales (DREI), Programme INRIA “Equipes Associées”, €60,000, January 2005 to December 2007. (Co-PI)
- “A Structural and Composable Framework for MP Systems,” Intel Corporation, \$135,000, September 2003.
- “Structural and Composable Performance Simulation of Complex Systems,” National Science Foundation, Next Generation Software (NGS) Program (CNS 0305617), \$1,101,503, September 2003 to August 2006. (PI with Malik, Pai, and Peh)
- Emerson Electric Co. E. Lawrence Keyes ’51 Award, \$30,000, June 2003.
- Xilinx Equipment Grant, \$46,300, June 2003.
- “Addressing The Mapping Problem,” Infineon Corporation, \$100,000, November 2003.
- “Optimization-Space Exploration,” Intel Corporation, \$53,000, March 2002.
- “Systematic Design-Space Exploration,” National Science Foundation, Faculty Early Career Development Award (CAREER) (CCF 0133712), \$357,130, January 2002 to December 2006. (Sole PI)
- “EPIC Compiler and Architecture Research,” Hewlett-Packard and Intel Corporation Itanium Processor Family Equipment Grant, \$64,960, November 2001. (Coordinated university wide grant of \$242,157.)
- “Analysis Tools for Network Processors,” IBM Corporation, \$30,000, June 2001.
- “Memory Shape and Flow Determination,” Intel Corporation, \$53,000, March 2001.
- “Modern Embedded Systems: Compilers, Architectures, and Languages (MESCAL),” Gigascale Silicon Research Center, \$350,000, January 2001 to December 2003. (Sole PI)
- “Ascertaining Runtime Branch Characteristics through Algebraic Analysis of Programs,” National Science Foundation, Information Technology Research (ITR) Program (CCF 0082630), \$310,000, September 2000 to August 2002. (PI with Clark and Skadron)

## OUTREACH

- Presenter of over a dozen STEM demonstrations to early elementary public school students. Students, teachers, and parents report that these demonstrations have made a significant impression on young students.

## UNIVERSITY SERVICE

- University Committee on Library and Computing, 2017-2020
- Committee on Discipline, 2016-2017
- Computer Science Class of 2018 BSE Advisor
- Princeton University Research Computing Advisory Group
- Computer Science Department’s Instructor Coordinator, 2014-2015
- Andlinger Center for Energy and the Environment Space Committee
- Computer Science Department’s Instructor Recruiting Committee, 2012-2015
- Princeton Institute for Computational Science and Engineering (PICSciE) Faculty Committee
- Computer Science Department’s Computing Infrastructure Advisory Group
- Computer Science Department’s Renovation Advisory Group
- Coordinator of various joint activities with the Department of Electrical Engineering
- Computer Science Department’s Diversity Task Force
- Class of 2004, 2005, 2006, 2007, 2008, 2009, 2014, 2015, 2016 Freshmen Advising
- Mathey College Faculty Fellow
- University Committee on Library and Computing, 2011-2014
- Associate Chair, Computer Science Department, 2007-2008
- University Committee on Examinations and Standing, 2006-2008
- University Committee on Committees, 2002-2005
- Computer Science Class of 2004 BSE Advisor

- School of Engineering and Applied Science *Ad Hoc* Committee on the Computing Requirement
- Co-leader School of Engineering and Applied Science Strategic Planning Executive Committee for Focus on the Faculty

## TEACHING

- COS-126: Introduction to Computer Science (Dean's letter of recognition for teaching)
- COS-217: Introduction to Programming Systems
- COS-320: Compiler Implementation
- COS-375: Introduction to Computer Architecture
- COS-598: Parallelism
- COS-598: Feedback-Directed Optimization
- COS-598: Computer Architecture Research Infrastructure Development
- COS-598: Synergistic Hardware-Compiler Architecture Design
- COS-598: Topics in Compiler Construction
- COS-598: Securing Hardware

## STUDENTS

### CURRENT DOCTORAL STUDENTS

Feng Liu (year 6), Stephen Beard (year 5), Jordan Fix (year 4), Nayana Prasad Nagendra (year 2), Hansen Zhang (year 2)

### COMPLETED DEGREES

Soumyadeep Ghosh

Ph.D. Thesis: TrustGuard: A Containment Architecture with Verified Output

First Position: Founder at Start-up

Heejin Ahn

Master of Engineering Degree

First Position: Google

Nick Johnson

Ph.D. Thesis: Static Dependence Analysis in an Infrastructure for Automatic Parallelization

First Position: D. E. Shaw Research

Taewook Oh

Ph.D. Thesis: Automatic Exploitation of Input Parallelism

First Position: Facebook

Thomas Jablin

Ph.D. Thesis: Automatic Parallelization for GPUs

First Position: University of Illinois

Prakash Prabhu

Ph.D. Thesis: Semantic Language Extensions for Implicit Parallel Programming

First Position: Google

Jialu Huang

Ph.D. Thesis: Automatically Exploiting Cross-Invocation Parallelism Using Runtime Information

First Position: Goldman Sachs

Hanjun Kim

Ph.D. Thesis: ASAP: Automatic Speculative Acyclic Parallelization for Clusters

First Position: Assistant Professor at Pohang University of Science and Technology

Arun Raman

Ph.D. Thesis: A System for Flexible Parallel Execution

First Position: Intel



Yun Zhang  
Ph.D. Thesis: Runtime Speculative Software-Only Fault Tolerance  
First Position: Goldman Sachs

Matthew Zoufaly  
Master of Engineering Degree  
First Position: Partner at Start-up

Jack Tzu-Han Hung  
Master of Engineering Degree  
First Position: Intel

Easwaran Raman  
Ph.D. Thesis: Parallelization Techniques with Improved Dependence Handling  
First Position: Google

Thomas Mason  
Master of Engineering Degree  
First Position: Johns Hopkins University Applied Physics Laboratory

Matthew Bridges  
Ph.D. Thesis: The VELOCITY Compiler: Extracting Efficient Multicore Execution from Legacy Sequential Codes  
First Position: Google

Bolei Guo  
Ph.D. Thesis: Shape Analysis with Inductive Recursion Synthesis  
First Position: JPMorgan

Neil Vachharajani  
Ph.D. Thesis: Intelligent Speculation for Pipelined Multithreading  
First Position: Google

Guilherme Ottoni  
Ph.D. Thesis: Global Instruction Scheduling for Multi-Threaded Architectures  
First Position: Intel Research

George A. Reis  
Ph.D. Thesis: Software Modulated Fault Tolerance  
First Position: Google

Ram Rangan  
Ph.D. Thesis: Pipelined Multithreading Transformations and Support Mechanisms  
First Position: IBM Austin Research Laboratory

Spyridon Triantafyllis  
Ph.D. Thesis: Eliminating Conventional Restrictions on Compiler Optimization  
First Position: D. E. Shaw Research

David A. Penry  
Ph.D. Thesis: Microarchitecture Modeling for Design-space Exploration  
First Position: Assistant Professor at Brigham Young University

Manish Vachharajani, co-advised with Sharad Malik  
Ph.D. Thesis: Microarchitecture Modeling for Design-space Exploration  
First Position: Assistant Professor at University of Colorado, Boulder

Jason Blome  
Master of Engineering Degree  
First Position: Ph.D. candidate at University of Michigan, Ann Arbor

## PUBLICATIONS

### BOOK CHAPTERS

- [1] David I. August, Jialu Huang, Thomas B. Jablin, Hanjun Kim, Thomas R. Mason, Prakash Prabhu, Arun Raman, and Yun Zhang, “Automatic Extraction of Parallelism from Sequential Code,” in *Fundamentals of Multicore Software Development* edited by Ali-Reza Adl-Tabatabai, Chapman Hall / CRC Press, December 2011. (ISBN: 978-1439812730)
- [2] Arun Raman and David I. August, “EPIC Processors,” in *Encyclopedia of Parallel Computing* edited by David Padua, Springer, November 2011. (ISBN: 978-0387098449)
- [3] David I. August, Veerle Desmet, Silvain Girbal, Daniel Gracia Prez, and Olivier Temam, “Structural Simulation for Architecture Exploration,” in *Processor and System-on-Chip Simulation* edited by Rainer Leupers and Olivier Temam, Springer, September 2010. (ISBN: 978-1441961747)
- [4] Neil Vachharajani and David I. August, “Speculation,” in *Encyclopedia of Computer Science and Engineering* edited by Benjamin W. Wah, John Wiley Sons, Inc., January 2009. (ISBN: 978-0471383932)
- [5] Easwaran Raman and David I. August, “Optimizations for the Memory Hierarchy,” in *Compiler Design Handbook* edited by Y. N. Srikant, CRC Press, December 2007. (ISBN: 978-1420043822)
- [6] David I. August, “Branch Predication,” in *Speculative Execution in High Performance Computer Architectures* edited by D. Kaeli and P.-C. Yew, CRC Press, May 2005. (ISBN: 978-1584884477)

### REFEREED JOURNAL PUBLICATIONS

- [7] Yun Zhang, Jae W. Lee, Nick P. Johnson, and David I. August, “DAFT: Decoupled Acyclic Fault Tolerance,” in *The International Journal of Parallel Programming (IJPP)*, February 2012. **Invited. Special issue composed of “top papers” selected by the Program Committee of the 19th International Conference on Parallel Architectures and Compilation Techniques.**
- [8] Arvind, David I. August, Keshav Pingali, Derek Chiou, Resit Sendag, and Joshua J. Yi, “Programming Multicores: Do Applications Programmers Need to Write Explicitly Parallel Programs?,” in *IEEE Micro*, May 2010.
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