David I. August

Curriculum Vitae

Contact Information

Department of Computer Science
Princeton University
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Princeton, NJ 08540

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Education

University of Illinois at Urbana-Champaign, Urbana, IL
Ph.D. in Electrical and Computer Engineering, May 2000
Thesis: "Systematic Compilation for Predicated Execution," Advisor: Wen-mei W. Hwu
M.S. in Electrical and Computer Engineering, May 1996
Advisor: Wen-mei W. Hwu

Rensselaer Polytechnic Institute, Troy, NY
B.S. in Electrical Engineering, Summa Cum Laude (1/1249), May 1993

Experience

Professor, July 2012 to Present; **Associate Professor**, July 2006 to June 2012; **Assistant Professor**, February 2000 to June 2006; **Lecturer**, August 1999 to January 2000
Department of Computer Science, *Princeton University*, Princeton, NJ

Consultant, August 1998-Present
Technology and intellectual property consulting

Research Intern, May to September 1996, November 1996
Intel Corporation, Santa Clara, CA

Research Intern, May to August 1995
Hewlett Packard Laboratories, Santa Clara, CA

Architecture Validation Engineer, May to August 1994
Intel Corporation, Hillsboro, OR

Recognition

- Elevation to IEEE Fellow "for contributions to compilers and architectures for multicore and parallel processing systems".
- Selection of "SWIFT: Software Implemented Fault Tolerance," for "The Test of Time Award" at The Thirteenth International Symposium on Code Generation and Optimization (CGO), 2015.
- Selection of "DAFT: Decoupled Acyclic Fault Tolerance" by the program committee for inclusion in special issue of *The International Journal of Parallel Processing* composed of "top papers" from the 19th International Conference on Parallel Architectures and Compilation Techniques (PACT), 2010.
- Nomination of "Fault-tolerant Typed Assembly Language" as a Communications of the ACM (CACM) Research Highlight, September 2008.
- Selection of "Revisiting the Sequential Programming Model for Multi-Core" for IEEE Micro's "Top Picks" special issue for papers "most relevant to industry and significant in contribution to the field of computer architecture" in 2007.
- Best Paper Award for "Fault-tolerant Typed Assembly Language" at the 2007 ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI), June 2007.
- Selection of "Automatic Instruction-Level Software-Only Recovery Methods" for IEEE Micro's "Top Picks" special issue for papers "most relevant to industry and significant in contribution to the field of computer architecture" in 2006.
- Selection of "Automatic Instruction-Level Software-Only Recovery Methods" for the William C. Carter Award at the International Conference on Dependable Systems and Networks, June 2006.

- Best Paper Award for "SWIFT: Software Implemented Fault Tolerance" at the Third Annual ACM/IEEE International Symposium on Code Generation and Optimization (CGO), March 2005.
- Emerson Electric Company E. Lawrence Keyes '51 Faculty Advancement Award, June 2003.
- Dean's letter of recognition for teaching, Spring 2003.
- Best Paper Award for "Compiler Optimization-Space Exploration" at the First Annual ACM/IEEE International Symposium on Code Generation and Optimization (CGO), March 2003.
- Best Student Paper Award for "Microarchitectural Exploration with Liberty" at the 35th Annual ACM/IEEE International Symposium on Microarchitecture (MICRO), November 2002.
- National Science Foundation Faculty Early Career Development Award (CAREER), 2002.
- Invited presentation at University of Virginia, *Top Gun Lecture Series* recognizing "faculty on a trajectory to be research leaders of the coming decades," December 2001.
- IBM Faculty Partnership Award, 2001-2002.
- Princeton University Research Board Award, 2001-2002.
- One of five featured by *The Chronicle of Higher Education* in its annual list of "New Ph.D.'s to Watch," September 1999.
- Selection of "A Framework for Balancing Control Flow and Predication" by the program committee for inclusion in special issue of *The International Journal of Parallel Processing* composed of "outstanding papers" from the 30th Annual ACM/IEEE International Symposium on Microarchitecture (MICRO), 1999.
- Intel Foundation Graduate Fellowship, 1996-1997.
- Department of Defense, Office of Naval Research Graduate Fellowship, 1993-1996.
- University of Illinois Henry O. Koehler Graduate Fellowship, 1993-1994.

Activities

Program Chair

- The 42nd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO) (with José Martínez, Cornell), 2009.
- The Fifth Annual International Symposium on Code Generation and Optimization (CGO) (with Chris J. Newburn, Intel), 2007.
- The IEEE International Conference on Computer Design (ICCD) - Computer Systems Design and Applications Track (with Mark Charney, Intel), 2003.
- The IEEE International Conference on Computer Design (ICCD) - Computer Systems Design and Applications Track (with Mark Charney, Intel), 2002.

Editing

- Guest Editor, IEEE Micro, special issue on "Parallelization of Sequential Code," July 2012.
- Editorial Board, IEEE Computer Architecture Letters, 2010 - 2014.
- Associate Editor, ACM Transactions on Architecture and Code Optimization, 2006 - present.
- Guest Editor, Computer Languages, Systems and Structures special issue on "Programming Language and Compiler Support for Secure and Reliable Computing," April 2006.

Technical Program Committees

- The CGO 2007 Test of Time Award Selection Committee, 2017
- The 22nd International Conference on Compiler Construction (CC), 2015
- The 41st Annual IEEE/ACM International Symposium on Computer Architecture (ISCA), 2014.
- IEEE MICRO Top-Picks in Computer Architecture, 2013.
- The ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI), 2013.
- IEEE MICRO Top-Picks in Computer Architecture, 2011.
- The Fourth Workshop on Parallel Execution of Sequential Programs on Multi-core Architectures (PESPMA), 2011
- The 11th International Symposium on Advanced Parallel Processing Technologies (APPT), 2011
- The First International Workshop on Future Architectural Support for Parallel Programming (FASPP), 2011
- The 16th International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), 2011.

- The 43rd Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), 2010.
- The Third Workshop on Emerging Applications and Many-core Architecture (EAMA), 2010.
- The Sixth Workshop on Modeling, Benchmarking and Simulation (MoBS), 2010.
- The First Workshop on Accelerators for High-performance Architectures (WAHA), 2009
- The Fifth IEEE International Symposium on Workload Characterization (IISWC), 2009.
- The ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI), 2008.
- IEEE MICRO Top-Picks in Computer Architecture, 2007.
- The Sixth Annual Workshop on Duplicating, Deconstructing, and Debunking (WDDD), 2007.
- The ACM International Conference on Computing Frontiers (CF), 2007.
- The 34th Annual IEEE/ACM International Symposium on Computer Architecture (ISCA), 2007.
- The 39th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), 2006.
- The International Conference on High Performance Embedded Architectures and Compilers (HiPEAC), 2006.
- The Workshop on Introspective Architectures (WISA), 2006.
- The 15th International Conference on Parallel Architectures and Compilation Techniques (PACT), 2006.
- The Second Workshop on Modeling, Benchmarking and Simulation (MoBS), 2006.
- The 10th Workshop on Interaction between Compilers and Computer Architectures (INTERACT), 2006.
- The IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2006.
- The 32nd Annual IEEE/ACM International Symposium on Computer Architecture (ISCA), 2005.
- The Workshop on Modeling, Benchmarking and Simulation (MoBS), 2005.
- The IEEE/ACM International Conference on Computer Aided Design (ICCAD), 2005.
- The International Conference on High Performance Embedded Architectures and Compilers (HiPEAC), 2005.
- The Third Annual International Symposium on Code Generation and Optimization (CGO), 2005.
- The International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES), 2004.
- The IEEE International Conference on Computer Design (ICCD) - Computer Systems Design and Applications Track, 2004.
- The IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2004.
- The Second Annual International Symposium on Code Generation and Optimization (CGO), 2004.
- The 30th Annual IEEE/ACM International Symposium on Computer Architecture (ISCA), 2003.
- The First Annual International Symposium on Code Generation and Optimization (CGO), 2003.
- The IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2003.
- The 35th Annual IEEE/ACM International Symposium on Microarchitecture (MICRO), 2002.
- The ACM Workshop on Languages, Compilers, and Tools for Embedded Systems (LCTES), 2002.
- The ACM International Conference on Measurement and Modeling of Computer Systems (SIGMETRICS), 2002.
- The 6th Workshop on Interaction between Compilers and Computer Architectures (INTERACT), 2002.
- The First Annual Workshop on Explicitly Parallel Instruction Computer Architectures and Compiler Technology (EPIC), 2001.
- The ACM Workshop on Languages, Compilers, and Tools for Embedded Systems (LCTES), 2001.
- The IEEE International Conference on Computer Design (ICCD), 2001.
- The 7th International IEEE Symposium on High-Performance Computer Architecture (HPCA), 2000.
- The IEEE International Conference on Computer Design (ICCD), 2000.

Conference Organizing and Steering Committees

- Steering Committee, The International Symposium on Code Generation and Optimization (CGO), 2007-2010.
- General Chair, The Fourth Annual International Symposium on Code Generation and Optimization (CGO), 2006.
- Publications Chair, The IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS), 2003.
- Finance Chair, The Second Annual International Symposium on Code Generation and Optimization (CGO), 2003
- General Chair, The Second Annual Workshop on Explicitly Parallel Instruction Computer Architectures and Compiler Technology (EPIC), 2002.

Technical Panels

- Panelist, "Advancing Computer Systems without Technology Progress," DARPA Information Science and Technology (ISAT) Workshop, March 2012.
- Panelist, "Freedom from the Tyranny of Parallel Programming," Workshop on Deterministic Multiprocessing and Parallel Programming (WoDet), November 2009.
- Panelist, "Programming for Multi-core Processors (OR NOT?)" Second Workshop on Computer Architecture Research Directions (CARD) held in conjunction with International Symposium on Computer Architecture (ISCA), June 2009.
- Panelist, "Are New Programming Languages Needed to Exploit Manycore Architectures?" Microsoft Research Faculty Summit, July 2007.
- Panelist, "Programming Languages/Models and Compiler Technologies," Manycore Computing Workshop held in conjunction with the International Conference on Supercomputing (ICS), June 2007.
- Panelist, "Are New Languages Necessary for Multicore," The Fifth International Symposium on Code Generation and Optimization (CGO), March 2007.
- Panelist, "Directions in Multi-Core Research," Microsoft Corporation, Redmond, WA, January 2007.
- Panelist, "What should architects know about compilers and systems software?" The Computing Research Association's Committee on the Status of Women (CRA-W) and the Coalition to Diversify Computing (CDC) Computer Architecture Summer School, 2006.
- Panelist, "Design Methodologies for Future Processor Chips," The Second Workshop on Modeling, Benchmarking and Simulation held in conjunction with the 33rd International Symposium on Computer Architecture (ISCA), 2006.
- Panelist, "Simulation Methodology," Third Annual Workshop on Duplicating, Deconstructing, and Debunking (WDDD) held in conjunction with International Symposium on Computer Architecture (ISCA), 2004.
- Panelist, "Emerging Issues with Simulation Technology" NSF-Sponsored Workshop, Austin, TX, December 2001.

Funding Panels

- National Science Foundation Secure and Trusted Cyberspace Panel (SaTC)
- National Science Foundation Software and Hardware Foundations Panel (SHF)
- National Science Foundation Computing Systems Research Panel (CSR) (2 times)
- National Science Foundation Computer Systems Architecture Panel (CSA)
- National Science Foundation Information Technology Research Panel (ITR)
- National Science Foundation Next Generation Software Panel (NGS)

Tutorials

- "Next Generation Automatic Parallelization," presented at the Eighth International Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems, Fiuggi, Italy, June 2012.
- "Fault Tolerant Computing," Summer School on Language-Based Techniques for Integrating with the External World, July 2007.
- "Structural Simulation," presented at the First International Summer School on Advanced Computer Architecture and Compilation for High-Performance and Embedded Systems, L'Aquila, Italy, June 2005.
- "Using The Liberty Simulation Environment with emphasis on validated OS-level simulation," presented at the 11th International Conference on Architectural Support for Programming Languages and Operating Systems in Boston, MA, October 2004.
- "The Liberty Simulation Environment, Version 1.0," presented at the 36th International Symposium on Microarchitecture in San Diego, CA, December 2003.
- "Architectural Exploration with Liberty," presented at the International Symposium on Microarchitecture in Austin, TX, December 2001.
- "Future Technologies and Markets for Programmable Platform-Based Design," presented at IP/SoC 2001 in Santa Clara, CA, March 2001.

Invited Talks

- Keynote: "Thoughts on Restoring Computing's Former Glory," presented at the 2012 Compiler, Archi-

tecture and Tools Day, Haifa, Israel, November 2012.
- Keynote: "Restoring Computing's Former Glory," presented at the 2012 Architecture of Computing Systems Conference, Munich, Germany, March 2012.
- "A Roadmap to Restoring Computing's Former Glory," presented at the HiPEAC Industrial Workshop, High-Performance and Embedded Computing, Charmonix, France, April 2011.
- Keynote: "Indistinguishable from Magic," presented at the 16th Workshop on Compiler Techniques for High-Performance and Embedded Computing, Taipei, Taiwan, May 2010.
- Keynote: "Parallelism for Multicore," presented at the 2009 Workshop on Parallel Execution of Sequential Programs on Multi-core Architectures held in conjunction with 36th International Symposium on Computer Architecture, June, 2009.
- "Parallelism for Multicore," presented at the New Jersey Programming Languages Seminar and Princeton Computer Architecture Research Day, March, 2009.
- "Addressing the Multicore Problem," presented at the Princeton Innovation Forum, March, 2009.
- "Automatic Thread Extraction from Sequential Programs," presented at Indian Institute of Science, March, 2008.
- "The Multicore Challenge," DARPA Information Processing Technology Office Futures Panel, December 2007.
- "Automatic Thread Extraction from Sequential Programs," presented at Microsoft Research Faculty Summit, 2007.
- "Liberating Threads from Sequential Programs," presented at Purdue University, November 2006.
- "The Jericho Project," presented at the Workshop on Design, Architecture and Simulation of Chip Multi-Processors, November 2005.
- "Liberating Threads from Sequential Programs," presented at Intel Microprocessor Laboratories, Hewlett-Packard Laboratories, Sun Microsystems Research Laboratories, INRIA Futurs, Cornell University, Carnegie Mellon University, and Massachusetts Institute of Technology, March-April 2005.
- "Liberating Threads from Sequential Programs," presented at the New Jersey Programming Languages Seminar, February 2005.
- "Liberty Compiler Research," presented at IBM T. J. Watson Research Center, April 2004.
- "Liberty Research," presented at Infineon Corporation and Aachen University, February 2004.
- "Architectural Exploration with Liberty," presented at the Intel High-Level Design Research Forum, November 2002.
- "Optimization-Space Exploration," presented at Intel Microprocessor Research Laboratories, Hewlett-Packard Laboratories, and Sun Microsystems Research Laboratories, August 2002.
- "Architectural Exploration with Liberty," presented at IBM T. J. Watson Research Center, July 2002.
- "Liberty Compiler and Architecture Research," presented at University of Texas at Austin, April 2002.
- "Architectural Exploration with Liberty," presented at University of Virginia, *Top Gun Lecture Series* recognizing "faculty on a trajectory to be research leaders of the coming decades," December 2001.
- "Architectural Exploration with Liberty," presented at Intel Microprocessor Laboratories, Hewlett-Packard Laboratories, and Sun Microsystems Research Laboratories, May 2001.
- "Architectural Exploration with Liberty," presented at University of Toronto, Distinguished Lecture Series, May 2001.
- "Systematic Compilation for Predicated Execution," presented at IBM Tokyo Research Laboratories, Rice University, and University of Illinois at Urbana/Champaign, January-August 2000.
- "Systematic Program Decision Logic Optimization Using Predication," presented at Intel Microprocessor Research Laboratories, April 1999.
- "Enabling Compiler Technology for Predication," presented at The Swiss Federal Institute of Technology of Lausanne (École Polytechnique Fédérale de Lausanne), February 1999.
- "Enabling Compiler Technology for Predication," presented at Compaq Corporation, November 1998.
- "A Global Predication Compilation Framework," presented at Microsoft Research, November 1998.
- "Predicated Microprocessor Architectures and Their Enabling Compiler Technology," presented at Silicon Graphics, February 1998.
- "Next Generation Predication Support in the IMPACT Compiler," presented at The Intel Foundation Fellowship Forum, November 1996.
- "Predicated Execution Architectures: New Research Results and Directions," presented at The Intel Microprocessor Research Forum, October 1995.

Grants

- "TrustGuard-secured Computing Devices," The Princeton University Intellectual Property Accelerator Fund, $100,000, January 2017. (Sole PI)
- "An Architecture for Restoring Trust in Our Personal Computing Systems," National Science Foundation, Secure and Trustworthy Cyberspace (SaTC) (CNS 1441650), $500,000, September 2014 to August 2017. (Sole PI)
- "A Framework for Portable Parallel Performance," National Science Foundation, Exploiting Parallelism and Scalability (XPS) (CCF 1439085), $300,000, August 2014 to July 2017. (Sole PI)
- "A Platform for Data-Parallel GPU Computing at Princeton," National Science Foundation, Computing Research Infrastructure (CRI) Program (CNS 1205613), $350,000, August 2012. (PI with 3 Co-PIs)
- "PRACTICE: Power-Reducing Adaptive Computing Technologies: Intelligent, Cross-layer, and Efficient," United States Department of Defense (DOD), Defense Advanced Research Projects Agency (DARPA), Power Efficiency Revolution For Embedded Computing Technologies (PERFECT) Program, $10,928,472, January 2012 to August 2015. (PI with 3 others)
- "A Platform for Data-Parallel GPU Computing at Princeton," National Science Foundation, Computing Research Infrastructure (CRI) Program (CNS 1205613), $350,000, August 2012. (PI with 3 Co-PIs)
- "Accelerating the Pace of Research (at Princeton)," Dean for Research Fund, $50,000, April 2012.
- "Automatic Parallelization for GPUs," NVIDIA Corporation Academic Partnership Award, $25,000, December 2010.
- "Accelerating the Pace of Research through Implicitly Parallel Programming," National Science Foundation, Software Infrastructure for Sustained Innovation Scientific (SI^2) Software Integration (SSI) Program (OCI 1047879), $1,740,314, October 2010 to September 2014. (PI with Walker)
- "Greater Philadelphia Innovation Cluster (GPIC) for Energy Efficient Buildings," United States Energy Regional Innovation Cluster (E-RIC) Initiative, $3,499,994 ($129,000,000 overall), October 2010 to September 2015. (Princeton University PI with 4 Co-PIs)
- "SPARCHS: Symbiotic, Polymorphic, Autotomic, Resilient, Clean-Slate, Host Security," United States Department of Defense (DOD), Defense Advanced Research Projects Agency (DARPA), Clean-slate design of Resilient, Adaptive, Secure Hosts (CRASH) Program, $6,424,180, September 2010 to September 2014. (PI with 4 others)
- "Scaling the Implicitly Parallel Programming Model with Lifelong Thread Extraction and Dynamic Adaptation," National Science Foundation, Computer Systems Research (CSR) Program (CNS 0964328), $1,199,998, May 2010 to April 2013. (PI with Hazelwood and Mahlke)
- "AESOP: Adaptive Environment for Supercompiling with Optimized Parallelism," United States Department of Defense (DOD), Defense Advanced Research Projects Agency (DARPA), Architecture-Aware Compiler Environment (AACE) Program, $11,572,332, September 2009 to January 2013. (PI with 4 others)
- "Implicitly Parallel Programming with Dynamic Execution," LG Electronics, $40,000, November 2009.
- "Hierarchical Latency and Throughput Optimization of Parallel Applications," Google Research Award, $50,000, November 2009.
- "A Hybrid Approach for Petascale Computing: Accelerating Scientific Research ," National Science Foundation, Small Grants for Exploratory Research (SGER) Program (OCI 0849512), $102,562, June 2009 to May 2010. (PI with Li and Ostriker)
- "Revisiting the Sequential Programming Model for Multicore Systems," National Science Foundation, Computing Processes and Artifacts (CPA) Program (CCF 0811580), $150,000, September 2008 to August 2009. (PI with Hazelwood and Mahlke)
- "Automatically Parallelizing Legacy Binary Code for Multi-Core Architectures via Extraction of Self-Similarity," United States Department of Defense (DOD), Defense Advanced Research Projects Agency (DARPA), $300,000, September 2008 to August 2009. (PI with Locasto, Sethumadhavan, and Stolfo)
- "Liberating Threads from Sequential Programs," Gigascale Silicon Research Center, $357,000, September 2006 to August 2009. (Sole PI)
- "Well-typed Trustworthy Computing in the Presence of Transient Faults," National Science Foundation, CyberTrust Program (CNS 0627650), $1,100,000, September 2006 to June 2010. (Co-PI with Walker, Appel, Clark, and Martonosi)
- "Software-Modulated Fault Tolerance," National Science Foundation, Computer Systems Research (CSR) Program (CNS 0615250), $320,000, July 2006 to June 2009. (Sole PI)
- "A Viable Approach to Compiling Sequential Codes for CMPs," Microsoft Corporation, $50,000, April

2006.
- "Flow-Based Computer Systems Support for Synergistic Hardware-Software Management of Embedded Systems," National Science Foundation, Computer Systems Research (CSR) Program (CNS 0509402), $500,000, September 2005 to August 2009. (Co-PI with Li, Martonosi, and Pe)
- "User-centric Information Flow Security," Intel Corporation, $120,000, August 2005 to July 2008.
- "Threading the CMP Needle with Fibers and Frays," The Microelectronics Advanced Research Corporation (MARCO), $122,500, April 2005 to August 2006. (Sole PI)
- "International Modular Simulation Research," Direction des Relations Européennes et Internationales (DREI), Programme INRIA "Equipes Associées", €60,000, January 2005 to December 2007. (Co-PI)
- "A Structural and Composable Framework for MP Systems," Intel Corporation, $135,000, September 2003.
- "Structural and Composable Performance Simulation of Complex Systems," National Science Foundation, Next Generation Software (NGS) Program (CNS 0305617), $1,101,503, September 2003 to August 2006. (PI with Malik, Pai, and Peh)
- Emerson Electric Co. E. Lawrence Keyes '51 Award, $30,000, June 2003.
- Xilinx Equipment Grant, $46,300, June 2003.
- "Addressing The Mapping Problem," Infineon Corporation, $100,000, November 2003.
- "Optimization-Space Exploration," Intel Corporation, $53,000, March 2002.
- "Systematic Design-Space Exploration," National Science Foundation, Faculty Early Career Development Award (CAREER) (CCF 0133712), $357,130, January 2002 to December 2006. (Sole PI)
- "EPIC Compiler and Architecture Research," Hewlett-Packard and Intel Corporation Itanium Processor Family Equipment Grant, $64,960, November 2001. (Coordinated university wide grant of $242,157.)
- "Analysis Tools for Network Processors," IBM Corporation, $30,000, June 2001.
- "Memory Shape and Flow Determination," Intel Corporation, $53,000, March 2001.
- "Modern Embedded Systems: Compilers, Architectures, and Languages (MESCAL)," Gigascale Silicon Research Center, $350,000, January 2001 to December 2003. (Sole PI)
- "Ascertaining Runtime Branch Characteristics through Algebraic Analysis of Programs," National Science Foundation, Information Technology Research (ITR) Program (CCF 0082630), $310,000, September 2000 to August 2002. (PI with Clark and Skadron)

Outreach

- Presenter of over a dozen STEM demonstrations to early elementary public school students. Students, teachers, and parents report that these demonstrations have made a significant impression on young students.

University Service

- Committee on Discipline
- Computer Science Class of 2018 BSE Advisor
- Princeton University Research Computing Advisory Group
- Computer Science Department's Instructor Coordinator, 2014-2015
- Andlinger Center for Energy and the Environment Space Committee
- Computer Science Department's Instructor Recruiting Committee, 2012-2015
- Princeton Institute for Computational Science and Engineering (PICSciE) Faculty Committee
- Computer Science Department's Computing Infrastructure Advisory Group
- Computer Science Department's Renovation Advisory Group
- Coordinator of various joint activities with the Department of Electrical Engineering
- Computer Science Department's Diversity Task Force
- Class of 2004, 2005, 2006, 2007, 2008, 2009, 2014, 2015, 2016 Freshmen Advising
- Mathey College Faculty Fellow
- University Committee on Library and Computing, 2011-2014
- Associate Chair, Computer Science Department, 2007-2008
- University Committee on Examinations and Standing, 2006-2008
- University Committee on Committees, 2002-2005
- Computer Science Class of 2004 BSE Advisor
- School of Engineering and Applied Science *Ad Hoc* Committee on the Computing Requirement

- Co-leader School of Engineering and Applied Science Strategic Planning Executive Committee for Focus on the Faculty

Teaching

- COS-126: Introduction to Computer Science (Dean's letter of recognition for teaching)
- COS-217: Introduction to Programming Systems
- COS-320: Compiler Implementation
- COS-375: Introduction to Computer Architecture
- COS-598: Parallelism
- COS-598: Feedback-Directed Optimization
- COS-598: Computer Architecture Research Infrastructure Development
- COS-598: Synergistic Hardware-Compiler Architecture Design
- COS-598: Topics in Compiler Construction
- COS-598: Securing Hardware

Students

Current Doctoral Students

Feng Liu (year 6), Stephen Beard (year 5), Jordan Fix (year 4), Nayana Prasad Nagendra (year 2), Hansen Zhang (year 2)

Completed Degrees

Soumyadeep Ghosh
Ph.D. Thesis: TrustGuard: A Containment Architecture with Verified Output
First Position: Founder at Start-up

Heejin Ahn
Master of Engineering Degree
First Position: Google

Nick Johnson
Ph.D. Thesis: Static Dependence Analysis in an Infrastructure for Automatic Parallelization
First Position: D. E. Shaw Research

Taewook Oh
Ph.D. Thesis: Automatic Exploitation of Input Parallelism
First Position: Facebook

Thomas Jablin
Ph.D. Thesis: Automatic Parallelization for GPUs
First Position: University of Illinois

Prakash Prabhu
Ph.D. Thesis: Semantic Language Extensions for Implicit Parallel Programming
First Position: Google

Jialu Huang
Ph.D. Thesis: Automatically Exploiting Cross-Invocation Parallelism Using Runtime Information
First Position: Goldman Sachs

Hanjun Kim
Ph.D. Thesis: ASAP: Automatic Speculative Acyclic Parallelization for Clusters
First Position: Assistant Professor at Pohang University of Science and Technology

Arun Raman
Ph.D. Thesis: A System for Flexible Parallel Execution
First Position: Intel

Yun Zhang
Ph.D. Thesis: Runtime Speculative Software-Only Fault Tolerance
First Position: Goldman Sachs

Matthew Zoufaly
Master of Engineering Degree
First Position: Partner at Start-up

Jack Tzu-Han Hung
Master of Engineering Degree
First Position: Intel

Easwaran Raman
Ph.D. Thesis: Parallelization Techniques with Improved Dependence Handling
First Position: Google

Thomas Mason
Master of Engineering Degree
First Position: Johns Hopkins University Applied Physics Laboratory

Matthew Bridges
Ph.D. Thesis: The VELOCITY Compiler: Extracting Efficient Multicore Execution from Legacy Sequential Codes
First Position: Google

Bolei Guo
Ph.D. Thesis: Shape Analysis with Inductive Recursion Synthesis
First Position: JPMorgan

Neil Vachharajani
Ph.D. Thesis: Intelligent Speculation for Pipelined Multithreading
First Position: Google

Guilherme Ottoni
Ph.D. Thesis: Global Instruction Scheduling for Multi-Threaded Architectures
First Position: Intel Research

George A. Reis
Ph.D. Thesis: Software Modulated Fault Tolerance
First Position: Google

Ram Rangan
Ph.D. Thesis: Pipelined Multithreading Transformations and Support Mechanisms
First Position: IBM Austin Research Laboratory

Spyridon Triantafyllis
Ph.D. Thesis: Eliminating Conventional Restrictions on Compiler Optimization
First Position: D. E. Shaw Research

David A. Penry
Ph.D. Thesis: Microarchitecture Modeling for Design-space Exploration
First Position: Assistant Professor at Brigham Young University

Manish Vachharajani, co-advised with Sharad Malik
Ph.D. Thesis: Microarchitecture Modeling for Design-space Exploration
First Position: Assistant Professor at University of Colorado, Boulder

Jason Blome
Master of Engineering Degree
First Position: Ph.D. candidate at University of Michigan, Ann Arbor

Publications

Book Chapters

[1] David I. August, Jialu Huang, Thomas B. Jablin, Hanjun Kim, Thomas R. Mason, Prakash Prabhu, Arun Raman, and Yun Zhang, "Automatic Extraction of Parallelism from Sequential Code," in *Fundamentals of Multicore Software Development* edited by Ali-Reza Adl-Tabatabai, Chapman Hall / CRC Press, December 2011. (ISBN: 978-1439812730)

[2] Arun Raman and David I. August, "EPIC Processors," in *Encyclopedia of Parallel Computing* edited by David Padua, Springer, November 2011. (ISBN: 978-0387098449)

[3] David I. August, Veerle Desmet, Silvain Girbal, Daniel Gracia Prez, and Olivier Temam, "Structural Simulation for Architecture Exploration," in *Processor and System-on-Chip Simulation* edited by Rainer Leupers and Olivier Temam, Springer, September 2010. (ISBN: 978-1441961747)

[4] Neil Vachharajani and David I. August, "Speculation," in *Encyclopedia of Computer Science and Engineering* edited by Benjamin W. Wah, John Wiley Sons, Inc., January 2009. (ISBN: 978-0471383932)

[5] Easwaran Raman and David I. August, "Optimizations for the Memory Hierarchy," in *Compiler Design Handbook* edited by Y. N. Srikant, CRC Press, December 2007. (ISBN: 978-1420043822)

[6] David I. August, "Branch Predication," in *Speculative Execution in High Performance Computer Architectures* edited by D. Kaeli and P.-C. Yew, CRC Press, May 2005. (ISBN: 978-1584884477)

Refereed Journal Publications

[7] Yun Zhang, Jae W. Lee, Nick P. Johnson, and David I. August, "DAFT: Decoupled Acyclic Fault Tolerance," in *The International Journal of Parallel Programming (IJPP)*, February 2012. Invited.
Special issue composed of "top papers" selected by the Program Committe of the 19th International Conference on Parallel Architectures and Compilation Techniques.

[8] Arvind, David I. August, Keshav Pingali, Derek Chiou, Resit Sendag, and Joshua J. Yi, "Programming Multicores: Do Applications Programmers Need to Write Explicitly Parallel Programs?," in *IEEE Micro*, May 2010.

[9] Ram Rangan, Neil Vachharajani, Guilherme Ottoni, and David I. August, "Performance Scalability of Decoupled Software Pipelining," in *ACM Transactions on Architecture and Code Optimization (TACO)*, August 2008.

[10] Matthew J. Bridges, Neil Vachharajani, Yun Zhang, Thomas B. Jablin, and David I. August, "Revisiting the Sequential Programming Model for the Multicore Era," in *IEEE Micro*, January 2008.
IEEE Micro's "Top Picks" special issue for papers "most relevant to industry and significant in contribution to the field of computer architecture" in 2007.

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[13] Manish Vachharajani, Neil Vachharajani, David A. Penry, Jason A. Blome, Sharad Malik, and David I. August, "The Liberty Simulation Environment: A Deliberate Approach to High-Level System Modeling," in *ACM Transactions on Computer Systems (TOCS)*, August 2006.

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[16] David I. August, Sharad Malik, Li-Shiuan Peh, Vijay Pai, Manish Vachharajani, and Paul Willmann, "Achieving Structural and Composable Modeling of Complex Systems," in *The International Journal of Parallel Programming (IJPP)*, June 2005. Invited.

[17] Spyridon Triantafyllis, Manish Vachharajani, and David I. August, "Compiler Optimization-Space Exploration," in *The Journal of Instruction-level Parallelism (JILP)*, February 2005.

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[21] Wen-mei W. Hwu, David I. August, and John W. Sias, "Program Decision Logic Optimization using Predication and Control Speculation," in *Proceedings of the IEEE*, November 2001.

[22] David I. August, Wen-mei W. Hwu, and Scott A. Mahlke, "The Partial Reverse If-Conversion Framework for Balancing Control Flow and Predication," in *International Journal of Parallel Programming (IJPP)*, October 1999. Invited.
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[23] Wen-mei W. Hwu, Richard E. Hank, David M. Gallagher, Scott A. Mahlke, Daniel M. Lavery, Grant E. Haab, John C. Gyllenhaal, and David I. August, "Compiler Technology for Future Microprocessors," in *Proceedings of the IEEE*, December 1995.

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[24] Nick P. Johnson, Jordan Fix, Taewook Oh, Stephen R. Beard, Thomas B. Jablin, and David I. August, "A Collaborative Dependence Analysis Framework," to appear in *Proceedings of the 2017 International Symposium on Code Generation and Optimization (CGO)*, February 2017.
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[25] Jialu Huang, Prakash Prabhu, Thomas B. Jablin, Soumyadeep Ghosh, Sotiris Apostolakis, Jae W. Lee, and David I. August, "Speculatively Exploiting Cross-Invocation Parallelism," in *Proceedings of the 25th International Conference on Parallel Architectures and Compilation Techniques (PACT)*, September 2016.

[26] Feng Liu, Heejin Ahn, Stephen R. Beard, Taewook Oh, and David I. August, "DynaSpAM: Dynamic Spatial Architecture Mapping using Out of Order Instruction Schedules," in *Proceedings of the 42nd International Symposium on Computer Architecture (ISCA)*, June 2015.

[27] Feng Liu, Soumyadeep Ghosh, Nick P. Johnson, and David I. August, "CGPA:Coarse-Grained Pipelined Accelerators," in *The Design Automation Conference (DAC)*, June 2014.

[28] Nick P. Johnson, Taewook Oh, Ayal Zaks, and David I. August, "Fast Condensation of the Program Dependence Graph," in *Proceedings of the 34th ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, June 2013.

[29] Taewook Oh, Hanjun Kim, Nick P. Johnson, Jae W. Lee, and David I. August, "Practical Automatic Loop Specialization," in *Proceedings of the Eighteenth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March 2013.

[30] Jialu Huang, Thomas B. Jablin, Stephen R. Beard, Nick P. Johnson, and David I. August, "Automatically Exploiting Cross-Invocation Parallelism Using Runtime Information," in *Proceedings of the 2013 International Symposium on Code Generation and Optimization (CGO)*, February 2013.

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[32] Daniel Schwartz-Narbonne, Feng Liu, David I. August, and Sharad Malik, "PASSERT: A Tool for Debugging Parallel Programs," in *Proceedings of the 18th International Conference on Computer-Aided Verification (CAV)*, June 2012.

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[35] Yun Zhang, Soumyadeep Ghosh, Jialu Huang, Jae W. Lee, Scott A. Mahlke, and David I. August, "Runtime Asynchronous Fault Tolerance via Speculation," in *Proceedings of the 2012 International Symposium on Code Generation and Optimization (CGO)*, April 2012.

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[37] Thomas B. Jablin, James A. Jablin, Prakash Prabhu, Feng Liu, and David I. August, "Dynamically Managed Data for CPU-GPU Architectures," in *Proceedings of the 2012 International Symposium on Code Generation and Optimization (CGO)*, March 2012.

[38] Kangkook Jee, Georgios Portokalidis, Vasileios P. Kemerlis, Soumyadeep Ghosh, David I. August, and Angelos D. Keromytis, "A General Approach for Efficiently Accelerating Software-based Dynamic Data Flow Tracking on Commodity Hardware," in *Proceedings of the 19th Internet Society (ISOC) Symposium on Network and Distributed Systems Security (NDSS)*, February 2012.

[39] Shantanu Gupta, Shuguang Feng, Amin Ansari, Scott A. Mahlke, and David I. August, "Bundled Execution of Recurring Traces for Energy-Efficient General Purpose Processing," in *Proceedings of the 44th IEEE/ACM International Symposium on Microarchitecture (MICRO)*, December 2011.
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[43] Prakash Prabhu, Soumyadeep Ghosh, Yun Zhang, Nick P. Johnson, and David I. August, "Commutative Set: A Language Extension for Implicit Parallel Programming," in *Proceedings of the 32nd ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, June 2011.

[44] Thomas B. Jablin, Prakash Prabhu, James A. Jablin, Nick P. Johnson, Stephen R. Beard, and David I. August, "Automatic CPU-GPU Communication Management and Optimization," in *Proceedings of the 32nd ACM SIGPLAN Conference on Programming Language Design and Implementation (PLDI)*, June 2011.

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Highest ranked paper in double-blind review process.

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[51] Easwaran Raman, Neil Vachharajani, Ram Rangan, and David I. August, "Spice: Speculative Parallel Iteration Chunk Execution," in *Proceedings of the 2008 International Symposium on Code Generation and Optimization (CGO)*, April 2008.

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[57] Bolei Guo, Neil Vachharajani, and David I. August, "Shape Analysis with Inductive Recursion Synthesis," in *Proceedings of the ACM SIGPLAN 2007 Conference on Programming Language Design and Implementation (PLDI)*, June 2007.

[58] Ram Rangan, Neil Vachharajani, Adam Stoler, Guilherme Ottoni, David I. August, and George Z. N. Cai, "Support for High-Frequency Streaming in CMPs," in *Proceedings of the 39th IEEE/ACM International Symposium on Microarchitecture (MICRO)*, December 2006.

[59] David Walker, Lester Mackey, Jay Ligatti, George A. Reis, and David I. August, "Static Typing for a Faulty Lambda Calculus," in *Proceedings of the 11th ACM SIGPLAN International Conference on Functional Programming (ICFP)*, September 2006.

[60] Jonathan Chang, George A. Reis, and David I. August, "Automatic Instruction-Level Software-Only Recovery," in *Proceedings of the International Conference on Dependable Systems and Networks (DSN)*, June 2006.
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[64] David A. Penry, Daniel Fay, David Hodgdon, Ryan Wells, Graham Schelle, David I. August, and Daniel A. Connors, "Exploiting Parallelism and Structure to Accelerate the Simulation of Chip Multiprocessors," in *Proceedings of the Twelfth International Symposium on High-Performance Computer Architecture (HPCA)*, February 2006.

[65] Guilherme Ottoni, Ram Rangan, Adam Stoler, and David I. August, "Automatic Thread Extraction with Decoupled Software Pipelining," in *Proceedings of the 38th IEEE/ACM International Symposium on Microarchitecture (MICRO)*, November 2005.
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[66] Guilherme Ottoni, Ram Rangan, Adam Stoler, and David I. August, "A New Approach to Thread Extraction for General-Purpose Programs," in *Proceedings of the 2nd Watson Conference on Interaction between Architecture, Circuits, and Compilers (PAC2)*, September 2005.

[67] George A. Reis, Jonathan Chang, Neil Vachharajani, Ram Rangan, David I. August, and Shubhendu S. Mukherjee, "Design and Evaluation of Hybrid Fault-Detection Systems," in *Proceedings of the 32nd International Symposium on Computer Architecture (ISCA)*, June 2005.

[68] Bolei Guo, Matthew J. Bridges, Spyridon Triantafyllis, Guilherme Ottoni, Easwaran Raman, and David I. August, "Practical and Accurate Low-Level Pointer Analysis," in *Proceedings of the Third International Symposium on Code Generation and Optimization (CGO)*, March 2005.

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[70] Neil Vachharajani, Matthew J. Bridges, Jonathan Chang, Ram Rangan, Guilherme Ottoni, Jason A. Blome, George A. Reis, Manish Vachharajani, and David I. August, "RIFLE: An Architectural Framework for User-Centric Information-Flow Security," in *Proceedings of the 37th International Symposium on Microarchitecture (MICRO)*, December 2004.

[71] Loukas Georgiadis, Renato F. Werneck, Robert E. Tarjan, Spyridon Triantafyllis, and David I. August, "Finding Dominators in Practice," in *Proceedings of the 12th European Symposium on Algorithms*, September 2004.

[72] Manish Vachharajani, Neil Vachharajani, Sharad Malik, and David I. August, "Facilitating Reuse in Hardware Models with Enhanced Type Inference," in *The IEEE/ACM/IFIP Second International Conference on Hardware/Software Codesign and System Synthesis (ISSS)*, September 2004.

[73] Ram Rangan, Neil Vachharajani, Manish Vachharajani, and David I. August, "Decoupled Software Pipelining with the Synchronization Array," in *Proceedings of the 13th International Conference on Parallel Architectures and Compilation Techniques (PACT)*, September 2004.
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Winner Best Paper Award.

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Winner Best Student Paper Award.

[79] Kaiyu Chen, Sharad Malik, and David I. August, "Retargetable Static Timing Analysis for Embedded Software," in *Proceedings of the 14th International Symposium on System Synthesis (ISSS)*, October 2001.

[80] John W. Sias, Wen-mei W. Hwu, and David I. August, "Accurate and Efficient Predicate Analysis with Binary Decision Diagrams," in *Proceedings of the 33rd International Symposium on Microarchitecture (MICRO)*, December 2000.

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[85] David I. August, Daniel A. Connors, John C. Gyllenhaal, and Wen-mei W. Hwu, "Architectural Support Compiler-Synthesized Dynamic Branch Prediction Strategies: Rationale and Initial Results," in *Proceedings of the Third International Symposium on High-Performance Computer Architecture (HPCA)*, February 1997.

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[87] Simha Sethumadhavan, Salvatore J. Stolfo, Angelos D. Keromytis, Junfeng Yang, and David I. August, "The SPARCHS Project: Hardware Support for Software Security," in *Proceedings of the First SysSec Workshop (SYSSEC)*, July 2011.

[88] Thomas B. Jablin, Yun Zhang, James A. Jablin, Jialu Huang, Hanjun Kim, and David I. August, "Liberty Queues for EPIC Architectures," in *Proceedings of the Eighth Workshop on Explicitly Parallel Instruction Computer Architectures and Compiler Technology (EPIC)*, April 2010.

[89] Guilherme Ottoni and David I. August, "Global Multi-Threaded Instruction Scheduling: Technique and Initial Results," in *Proceedings of the Sixth Workshop on Explicitly Parallel Instruction Computer Architectures and Compiler Technology (EPIC)*, March 2007.

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[96] Easwaran Raman and David I. August, "Recursive Data Structure Profiling," in *Proceedings of the Third Annual ACM SIGPLAN Workshop on Memory Systems Performance (MSP)*, June 2005.

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[99] Spyridon Triantafyllis, Manish Vachharajani, and David I. August, "Procedure Boundary Elimination for EPIC Compilers," in *Proceedings of the Second Workshop on Explicitly Parallel Instruction Computer Architectures and Compiler Technology (EPIC)*, November 2002.

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